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PAPER

Doping dependent crystal structures and optoelectronic properties of n-type CdSe:Ga nanowries†

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Although CdSe nanostructures possess excellent electrical and optical properties, efforts to make nano-optoelectronic devices from CdSe nanostructures have been hampered by the lack of efficient methods to rationally control their structural and electrical characteristics. Here, we report CdSe nanowires (NWs) with doping dependent crystal structures and optoelectronic properties by using gallium (Ga) as the efficient n-type dopant *via* a simple thermal co-evaporation method. The phase change of CdSe NWs from wurtzite to zinc blende with increased doping level is observed. Systematical measurements on the transport properties of the CdSe:Ga NWs reveal that the NW conductivity could be tuned in a wide range of near nine orders of magnitude by adjusting the Ga doping level and a high electron concentration up to 4.5×10^{19} cm^{-3} is obtained. Moreover, high-performance top-gate field-effect transistors are constructed based on the individual CdSe:Ga NWs by using high-κ HfO_2 as the gate dielectric. The great potential of the CdSe:Ga NWs as high-sensitive photodetectors and nanoscale light emitters is also exploited, revealing the promising applications of the CdSe:Ga NWs in new-generation nano-optoelectronics.

1. Introduction

II–VI nanostructures have attracted considerable attention in the past decade owing to their unique optical and electrical properties.[1,2] They are potential high-performance building blocks for new-generation nanoelectronic and nano-optoelectronic devices. So far, various nanodevices such as nano-field-effect transistors (nanoFETs), nanophotoswitches, nano-light emitting diodes (nanoLEDs), nano-laser diodes (nanoLDs), and solar cells have been realized by using the II–VI nanostructures as the functional components.[3–6] In spite of these progresses, the practical applications of the II–VI nanostructures are still obstructed by the difficulty in rationally controlling their transport properties as well as their crystal structures.[2]

As one of the most important II–VI semiconductors, cadmium selenium (CdSe) nanostructures have been intensively studied and much effort has been devoted to grow CdSe nanostructures *via* various methods.[7–11] However, the intrinsic CdSe nanostructures normally exhibit poor electrical conductivity due to the low carrier concentration arising from the high crystal quality of the nanostructures and therefore are not suitable for the nano-optoelectronic applications.[1] To promote their device applications, appropriate n- and p-type doping to the CdSe nanostructures are much desired in further research. On the other hand, it is known that the electronic structures of the semiconductor are determined by its crystal phase as well. For instance, the band gap of SiC is 3.33 eV for the wurtzite phase,[12] in contrast to 2.42 eV for the zinc blende phase,[13] hence the capability to control the phase structures of the CdSe nanostructures is also essential to their practical applications.

Herein, we demonstrated the successful synthesis of gallium (Ga) doped n-type CdSe nanowires (NWs). It is found that the Ga doping level played an important role in determining the crystal structures as well as the transport properties of the NWs. High-performance nanodevices, including top-gate nanoFETs, nano-photodetectors, and nanoLEDs, were then realized based on the CdSe:Ga NWs, revealing the promising applications of the CdSe:Ga NWs in future nano-optoelectronics.

2. Experimental

2.1 Material synthesis

Ga-doped CdSe NWs were synthesized in a horizontal tube furnace *via* a thermal co-evaporation method. Although the melting point of elementary gallium is very low, its boiling point is too high (~2100 °C) to be evaporated even at a high temperature excess 1000 °C, hence our primary attempt using elementary

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gallium as the doping source was failure. To address this issue, Ga and Ga_2O_3 mixed powder was used as the dopant source instead in this work. Ga vapor could be generated through the following reactions at relative low temperature (>600 °C):

$$4Ga\ (l) + Ga_2O_3\ (s) \rightarrow 3Ga_2O\ (g) \quad (1)$$

$$Ga_2O\ (g) + H_2\ (g) \rightarrow 2Ga\ (g) + H_2O\ (g) \quad (2)$$

The vapor pressure of Ga depends on the reaction temperature, thus allowing us to adjust the Ga doping level in the CdSe NWs by simply changing the evaporation temperature.[14,15] In detail, 0.2 g CdSe, Ga, and Ga_2O_3 mixed powder was used as the evaporation source and placed at the center region of the tube furnace. The content of Ga and Ga_2O_3 in the evaporation source was 8 wt% and the molar ratio of Ga:Ga_2O_3 was 4:1. Si substrates coated with 10 nm Au catalyst were placed at the downstream position ~12 cm from the evaporation source. Ar and H_2 (5%) mixed gas was used as the carrier gas with a constant flow ratio of 60 sccm. The pressure in the tube was adjusted to 150 Torr during the experiments and growth duration was 2 hours. In this work, three samples marked by N1, N2, and N3 with varied Ga doping level were synthesized, according to the increased source evaporation temperature of 795, 845 and 895 °C, respectively. Undoped CdSe NWs were also synthesized under the same conditions except the use of the Ga dopant for comparison, which were marked as N0.

2.2 Material characterizations

The structures, morphologies and compositions of those samples were characterized by X-ray diffraction (XRD,X'Pert with Cu K_α radiation), field-emission scanning electron microscopy (FESEM, Sirion 200 FEG), high-resolution transmission electron microscopy (Philips CM200FEG operated at an accelerating voltage of 200 kV), and X-ray photoemission spectroscopy (Thermo ESCALAB 250). Raman spectra were obtained by using 514.5 nm excitation laser (LabRAM-HR). Room-temperature photoluminescence (PL) spectra were measured with 325 nm laser excitation.

2.3 Device fabrication and analysis

To assess the electrical properties of the CdSe:Ga NWs, two types of field-effect transistors (FETs), including the back-gate FETs and top-gate FETs, were constructed based on the individual CdSe NWs. To fabricate the back-gate FETs, the as-synthesized CdSe NWs were first dispersed on a SiO_2 (300nm)/p+−Si substrate, and subsequently photolithography and lift-off processes were used to define In (100 nm) source and drain electrodes on the NWs. The degenerately doped Si substrate then acted as the global back gate. As for the top-gate FETs, 30 nm HfO_2 gate dielectric was grown by the atomic layer deposition (ALD Cambridge NanoTech), followed by the fabrication of the Ti/Au top-gate. All the electrical measurements were conducted at room temperature with a semiconductor characterization system (Keithley 4200-SCS). White light from the optical microscopy on the probe station was used as the light source for the detection of the photoconductive properties of the CdSe:Ga NWs.

3. Results and discussion

Fig. 1a shows the typical FESEM image of the Ga-doped CdSe NWs. It is seen that the wire-like product is clean and uniform and free of evident impurities and particles. The diameter and length of the NWs are in the range of 50–300 nm and 15–100 μm, respectively. The CdSe:Ga NWs are selectively grown on the Au catalyst coated area (Fig. 1b), and the Au catalyst caps could be clearly observed on the tips of the NWs, revealing the vapor-liquid-solid (VLS) growth mechanism of the NWs. The change in crystal phase is observed from the XRD patterns of the samples (Fig. 1d); the phase of the undoped CdSe NWs (N0) is wurtzite (JCPDS 77-2307), while it changes to zinc blende (JCPDS 88-2346) for N1, and to wurtzite again for N2 and N3. No detectable impurity peaks present in the XRD pattern, indicating the high crystal purity of the product. XPS detections on the samples reveal that only N3, which has the highest doping level, shows an evident Ga 2p3 signal at ~1118 eV with an estimated Ga content of ~1.2 at.% (Fig. 1e). In contrast, no Ga signal could be detected for other samples, implying the Ga content in these samples should be lower than 1% (XPS sensitivity limitation). However, for a semiconductor, it is known that small amount of element doping, even less than 0.1%, is already high enough to result in the dramatic change of its electrical transport properties. The detailed influence of doping on the transport properties of the CdSe NWs will be discussed later.

The crystal structures of the CdSe:Ga NWs were further evaluated by the TEM investigation, as shown in Fig. 2. Fig. 2a and d show the low-resolution TEM images of N1 and N3, respectively. The CdSe:Ga NWs with different doping level have similar one-dimensional morphology except the difference in the growth tips; a ball shape Au catalyst cap is observed for N1,

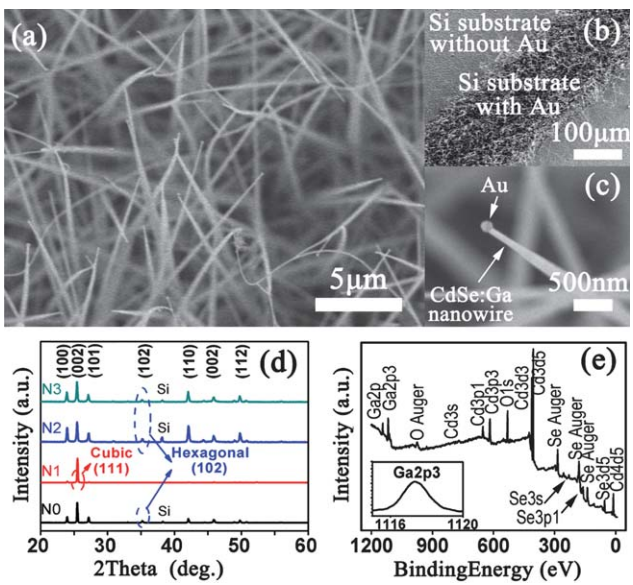

Fig. 1 (a) Typical SEM image of CdSe:Ga NWs. (b) SEM image shows the localized growth of CdSe:Ga NWs on the Au coated region. (c) Enlarged SEM shows the CdSe:Ga NW with a Au catalyst tip on the top of the NW. (d) XRD patterns of the samples. From bottom to top are N0, N1, N2, and N3, respectively. (e) XPS survey spectrum of the CdSe:Ga NWs (collected from N3). Inset shows the enlarged Ga2p3 peak.

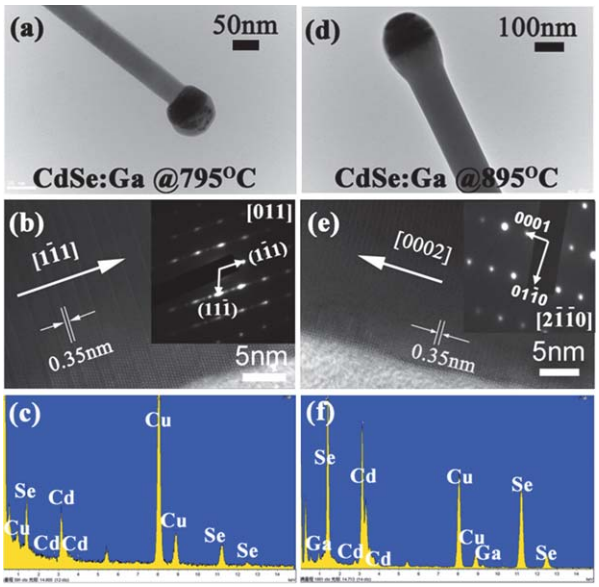

Fig. 2 (a) SEM image, (b) HRTEM image, and (c) EDS spectrum of N1. Inset in (b) shows the SAED pattern of N1. (d) SEM image, (e) HRTEM image, and (f) EDS spectrum of N3. Inset in (e) shows the SAED pattern of N3.

while it changes to half-ball shape for N3. HRTEM investigation reveals that N1 has cubic zinc blende structure with [1–11] growth orientation (Fig. 2b), in contrast to the hexagonal wurtzite structure for N3 with [0002] orientation (Fig. 2e). Because of the incorporation of Ga impurities, layer faults and twin structures are often observed in N1, which is reflected in its SAED pattern (inset in Fig. 2b). On the other hand, no Ga element could be detected in the energy dispersive X-ray (EDX) spectrum of N1 (Fig. 2c), while the EDX spectrum of N3 shows the presence of ~1.9 at.% Ga in the NW. These results are in well agreement with the XRD and XPS detections mentioned above.

To clarify the roles of the Ga doping level and the growth conditions on the morphologies and structures of the CdSe:Ga NWs, controlled experiments were performed (see Supporting Information, Fig. 1S). It is found that the intrinsic CdSe NWs have wurtzite structure no matter what experiment temperature is used. Therefore, we can conclude that the phase change for N1 at source evaporation temperature of 795 °C is most likely caused by the incorporation of Ga atoms, while at higher experiment temperature of 845 and 895 °C, it seems that the temperature instead of the Ga doping has dominated the NW crystal phase. These results could be qualitatively interpreted in terms of the liquid catalyst alloy/solid CdSe NW interfacial energy and CdSe NW surface energy.[16] The formation of Au-Cd-Ga ternary liquid phase for the catalyst alloy may lead to the variation of the surface energy of the Au-Cd-Ga (liquid)/Cd-Ga (solid) interface. Although wurtzite CdSe nanostructures are obtained in most occasions because it is the energy stable phase, the energy difference between the zinc blende phase and the wurtzite phase is very small in fact, hence the variation of the surface energy may result in the growth of the zinc blende NWs. At higher growth temperature, however, temperature plays a more important role, thus stable wurtzite CdSe NWs are obtained. On the other hand, it is seen that the intrinsic NWs have the same tip shapes with that of Ga-doped NWs at different temperature (see Supporting Information, Fig. 2S), indicating that the tip shapes are mainly controlled by the experiment temperature. The decreased viscosity of the Au catalyst droplets and the improved wettability of the Au droplets to the CdSe NWs might be responsible for the more flat (half-ball) catalyst tips at higher temperature.

Fig. 3a depicts the Raman spectra of the samples. Scattering peaks located at 204 and ~408 cm^{-1} are presented for all the samples and can be assigned to CdSe with 1LO and 2LO longitudinal optical phonon modes, respectively.[17,18] It is noted that the 2LO peaks shift slightly from 411 cm^{-1} to 408 cm^{-1}, along with the decrease of the peak intensity, as the doping level is gradually increased. The red-shift of the 2LO peak from N0 to N1 may reflect the phase change of the NWs from wurtzite to zinc blende, which is consistent with previous report.[19] However, the further decrease of the wavelength number for N2 and N3 is likely caused by the enhanced lattice strain in the CdSe NWs due to the incorporation of the Ga^{3+} ions, whose ionic radius (0.62 Å) is much smaller than that of the Cd^{2+} ions (0.97 Å). On the other hand, the decrease of the Raman intensity could be ascribed to the enhanced disorder in the CdSe NW upon Ga doping. The optical properties of the CdSe:Ga NWs is further investigated by PL spectra, as shown in Fig. 3b. The emission band of the undoped CdSe NWs is centered at 718 nm, which corresponds to the near band-edge (NBE) emission of CdSe. Nevertheless, the emission bands tend to shift to the longer wavelength direction and center at 742nm, 746nm and 751nm for N1, N2, and N3, respectively, with the increasing of the doping level. In addition, the emission intensity also gradually decreases from N0 to N3,

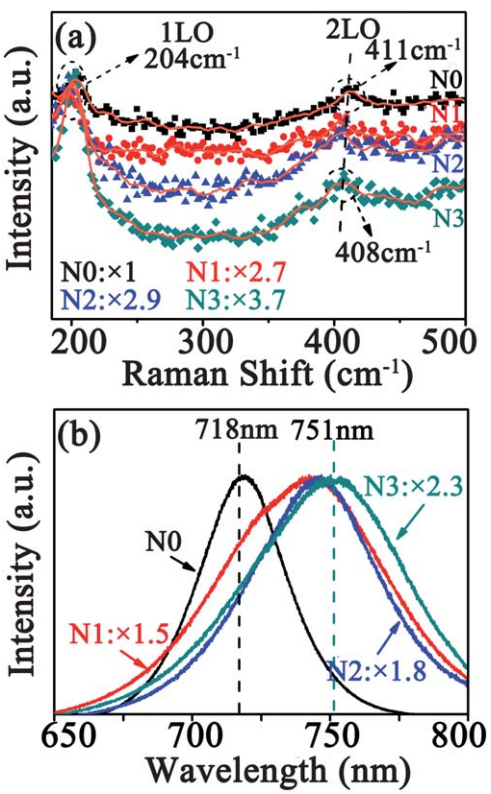

Fig. 3 (a) Raman spectra and (b) PL spectra for both undoped and Ga-doped CdSe NWs.

along with the obvious increase of the full-width at half-maximum (FWHM) of the emission bands (38 nm for N0, and 69 nm for N3). The broadening of the emission bands can be interpreted by the formation of band tailing in the band gap, which is often induced by the introduction of impurity into the semiconductor. On the other hand, the narrowing of the NW band-gap upon Ga doping also leads to the red-shift of the emission bands. The PL spectra provide a clear evidence of the successful Ga doping in the CdSe NWs.

In order to assess the electrical transport properties of the CdSe:Ga NWs, back-gate FETs based on the individual NWs were constructed (see the Supporting Information, Fig. 3S). The doping effects were first determined by measuring the conductance of the samples. Inset in Fig. 4a shows the typical *I–V* curve of the undoped CdSe NW (N0), which is measured under light illumination since almost no current could be detected in dark. It is seen that the NW is highly insulating with resistance as high as 9.6×10^{10} Ω. In contrast, the Ga-doped CdSe NWs show large conductance even in dark (Fig. 4a). The linear shape of the *I–V* curves indicate the excellent ohmic contact of the In electrodes with the CdSe:Ga NWs. The resistances of the NWs have decreased dramatically to 6.9×10^5 Ω, 2.9×10^4 Ω, and 3.0×10^3 Ω for sample N1, N2, and N3, respectively. To gain statistical significance, we measured the conductivity of 20–30 NWs for each sample and the corresponding conductivity distribution is depicted in Fig. 4b. Significantly, the conductivity of the CdSe NW could be tuned in a wide range of about nigh orders of magnitude from ~10^{-7}–10^{-6} Scm^{-1} for N0 (in light) to ~0.1–15 Scm^{-1} for N1, ~10–90 Scm^{-1} for N2, and ~40–350 Scm^{-1} for N3. These results unambiguously demonstrate that the efficient Ga doping has been realized in the CdSe NWs. The ability to tune the electrical properties of the CdSe NWs is vital to their potential applications in nanoelectronics and nano-optoelectronics.[20–27] Our success makes an important step towards the practical applications of the CdSe nanostructures.

Although the CdSe:Ga NWs show good *I–V* characteristics, their back-gate FETs exhibit poor gating effect even at a large gate voltage range of ±45 V (see the Supporting Information, Fig. 3S). The weak gate/channel coupling, which is an inherent deficiency for the back-gate device structure, is suggested to be responsible for the poor device performance. To improve the FET performance, top-gate FETs with high-κ HfO_2 ($\varepsilon = 17.7$) dielectric were fabricated from the CdSe:Ga NWs. Instead of the thick SiO_2 dielectric, 30 nm HfO_2 thin film was used as the gate insulator, and the NW channel could be modulated by the localized Ti/Au gate electrode. The top gate surrounds the NW conduction channel with a "Ω" shape, further enhancing the gate coupling. Fig. 5b–d depict the typical source-drain current (I_{ds}) *versus* source-drain voltage (V_{ds}) curves measured at varied gate voltage (V_G) for the top-gate NW FETs. It is seen that the devices exhibit much improved device performances as compared with the back-gate FETs. The conductances of the NWs can be effectively modulated under a relative low gate voltage (±4 V for N1, ±18 V for N2 and N3), and increase with the increasing of the gate voltage, revealing the n-type nature of the Ga-doped CdSe NWs. From the I_{ds}-V_G curves (insets in Fig. 5b–d), it is seen that the threshold voltages (V_{th}) for N1, N2 and N3 are −1 V, −16 V, and −102 V, respectively. The decrease of V_{th} is a result of the increased carrier concentration from N1 to N3 so that a smaller voltage is needed to turn on the conduction channel. Moreover, the electron mobility (μ) can be deduced from the transconductance (g_m) of the top-gate FETs. In the linear regime of the I_{ds}- V_G curve,

$$g_m = \frac{dI_{ds}}{dV_g} = \frac{\mu C V_{ds}}{L^2} \quad (3)$$

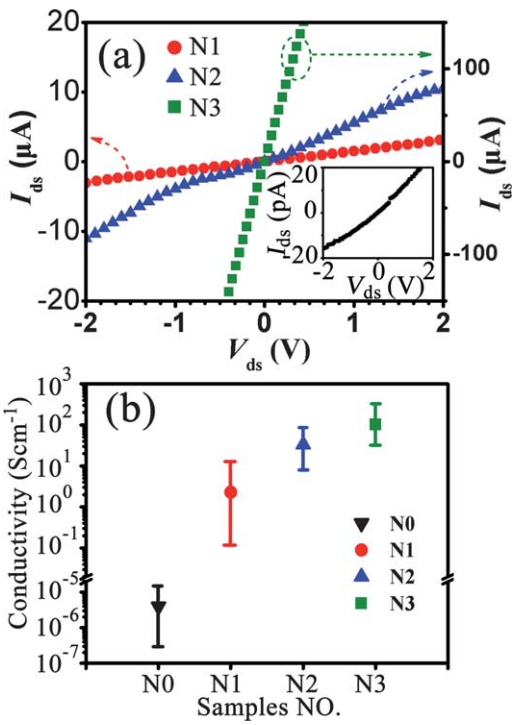

Fig. 4 (a) *I–V* characteristics of CdS:Ga NWs with varied doping levels. Inset shows the *I–V* curve of the undoped CdSe NW. (b) Distribution of conductivity values for N0, N1, N2, and N3.

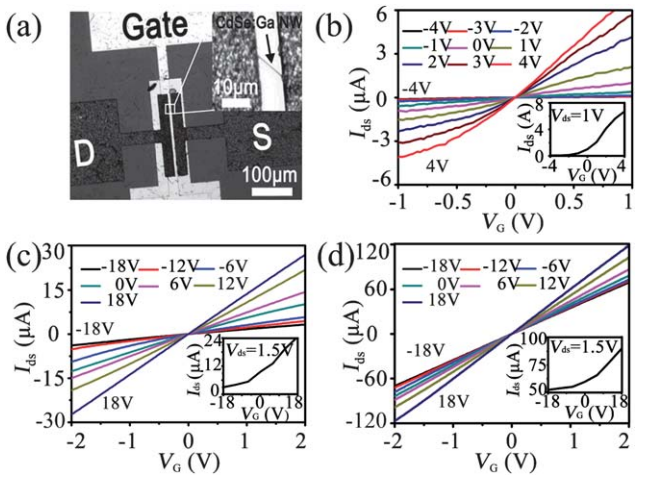

Fig. 5 (a) SEM image of the top-gate nanoFET fabricated from single CdSe:Ga NW. Inset shows the enlarged SEM image of the NW channel. (b), (c) and (d) are the electrical transport characteristics of the top-gate nanoFETs fabricated from N1, N2, and N3, respectively. I_{ds}-V_{ds} curves were plotted at varied V_G. Insets show the I_{ds}-V_G curves measured at fixed V_{ds}.

where C is the capacitance and L is the length of the active NW channel. The capacitance is given by

$$C = 2\pi\varepsilon_0\varepsilon_{HfO_2}L/\ln(1 + 2h/d) \quad (4)$$

where ε_{HfO_2} is the dielectric constant of HfO_2, h the thickness of the dielectric layer, and d the NW diameter. Based on the above equations, the mobility of N1, N2 and N3 are estimated to be about 8.2 $cm^2V^{-1}s^{-1}$, 10.5 $cm^2V^{-1}s^{-1}$, and 14.8 $cm^2V^{-1}s^{-1}$, respectively. The increased electron mobility from N1 to N3 is likely due to the improved electrode contact with the increasing of the doping level. The carrier concentration (n) in the CdSe:Ga NWs could be deduced to be 4.7×10^{18} cm^{-3} for N1, 1.5×10^{19} cm^{-3} for N2, and 4.5×10^{19} cm^{-3} for N3, respectively, according to the following relationship:

$$n = \sigma/\mu q \quad (5)$$

where σ is the conductivity of the NW, and q is the elementary charge. Such a high doping concentration in the CdSe:Ga NWs further indicates that Ga could be an very efficient n-type dopant for tuning the transport properties of the CdSe nanostructures. Based on the above results, we can conclude that Ga atoms were incorporated into the CdSe NWs *via* substituting the Cd atoms. The excess outer-shell electron of Ga is responsible for the n-type characteristics of the doped NWs.

CdSe nanostructures are promising candidates for nano-optoelectronic applications, such as solar cells, photodetectors, and nano-light emitters. We have conducted the preliminary studies on the optoelectronic applications of the CdS:Ga NWs in this work. Fig. 6 shows the photoresponse of the NWs under the white-light illumination (0.3 $mWcm^{-2}$). All the samples exhibit obvious photoresponse to the incident light with a reasonable response speed as well as excellent reproducibility and stability. Responsivity (R), which represents the sensitivity of a photodetector to the incident light, is defined as:

$$R(A/W) = \frac{I_p}{P_{opt}} = \eta\left(\frac{q\lambda}{hc}\right)G \quad (6)$$

$$G = \frac{N_{el}}{N_{ph}} = \frac{\tau}{\tau_{tr}} \quad (7)$$

where I_p is the photocurrent, P_{opt} the incident light power, η the quantum efficiency, h Planck's constant, c the light speed, λ the incident light wavelength, and G the photoconductive gain, which is defined as the ratio between the number of electrons collected per unit time (N_{el}) and the number of absorbed photons per unit time (N_{ph}) or the ratio of carrier lifetime (τ) to carrier transit time (τ_{tr}). Based on the above equations, R is estimated to be 5.6 AW^{-1} for N0, 1×10^6 AW^{-1} for N1, 5×10^5 AW^{-1} for N2, and 9×10^5 AW^{-1} for N3. For the doped samples, R values are in the same order and show little dependence on the doping level. By assuming $\eta = 1$ for simplification and using the central wavelength of the LED light at 470 nm, the photoconductive gain could be calculated, which has significantly increased from 14.4 for N0 to 2.6×10^6 for N1. The substantial improvement of R and G for the CdSe:Ga NWs could be attributed to (i) the improved ohmic contact for doped NWs, leading to a higher photocurrent. (ii) the presence of deep level trap states in NWs, which greatly prolong the lifetime of photo-carriers by preventing the electron-hole recombination.[28] Our results demonstrate that the photoconductive properties of the CdSe NWs can be dramatically enhanced by the Ga doping.

NanoLEDs based on the CdSe:Ga NWs were fabricated by using a heterojunction structure, which combines the n-type NWs and the p-type Si substrate, as shown in Fig. 7. First of all, SiO_2/p^+-Si substrate was HF etched to define the square SiO_2 insulating islands on the p^+-Si substrate (0.002–0.01 Ωcm). Then the CdSe:Ga NWs were dispersed on the substrate, followed by the photolithography and lift-off processes to fabricate the square In electrode pads on the SiO_2 islands. P-n junctions were formed at the contact region of the CdSe:Ga NWs with the p^+-Si substrate. This n-CdSe NW/p^+-Si substrate heterojunction shows excellent rectification behavior with a small turn-on voltage of ~1.2 V. At a low forward bias (+4 V), a bright emitting spot with red color could be clearly observed by naked eyes from the optical microcopy (right inset in Fig. 7). In contrast, no p-n junction could be obtained if the undoped CdSe NWs were used.

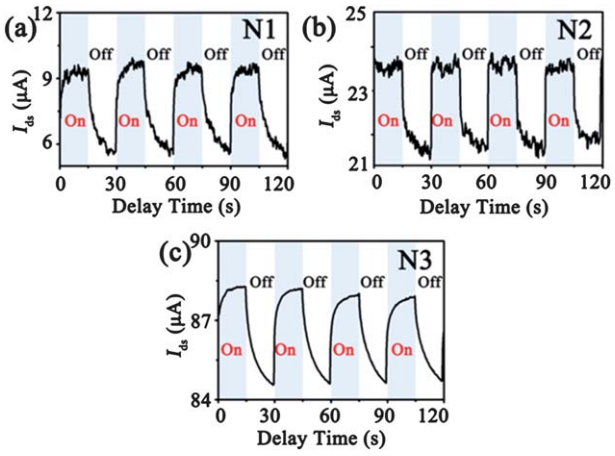

Fig. 6 Time response of (a) N1, (b) N2, and (c) N3. White light from the optical microscope was turned on/off manually. V_{ds} was fixed at +2 V.

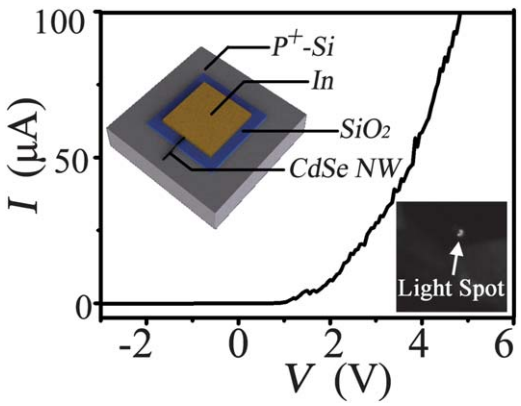

Fig. 7 Rectification characteristic of the n-CdSe NW/p+−Si heterojunction. Left inset shows the schematic illustration of the device. Right inset shows the optical image of the nanoLED. A red-light spot could be observed at the contact region of the n-CdSe:Ga NW with the p+−Si substrate at forward work bias.

4. Conclusions

In summary, we demonstrate the successful tuning of the crystal structures and the optoelectronic properties of the CdSe NWs by *in-situ* gallium doping *via* a simple thermal co-evaporation method. It is found that morphologies, structures, and optical properties of the CdSe NWs are dominated by the Ga doping. Successful Ga doping in the CdSe NWs is certified by the XPS, EDX, PL, and in particular, electrical measurements. The conductivity of the CdSe NWs could be tuned in a wide rang of near nine orders of magnitude by simply varying the growth temperature. Top-gate high-κ NW FETs based on the CdSe:Ga NWs show pronounced n-type gating effect and a high electron concentration up to 4.5×10^{19} cm^{-3} is revealed. Moreover, the doped NWs exhibit a high sensitivity to the incident light with a large photoconductive gain. NanoLEDs is also realized by using n-CdSe NW/p^+−Si substrate heterojunctions. It is expected that the CdSe:Ga NWs with tunable structural and optoelectronic properties will have important applications in new-generation nano-optoelectronic devices.

Acknowledgements

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