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Silicon Microwires Arrays: Synthesis, Mechanism, and Electrical Property

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ABSTRACT

Wafer-scale uniform silicon microwires (SiMWs) arrays were fabricated via gold-assisted chemical etching of silicon wafers. The diameter of SiMWs can be precisely controlled by etching duration and over-developing the patterned photoresist dots, so that SiMWs with diameters of 2.5, 2.0, 1.5, 1.0 and 0.6 μm were readily obtained. The etching direction was always vertical to the wafer surface, thus SiMWs with a direction along, [100] [110], [111] and [311] were readily fabricated from wafers of the corresponding orientation. The gold-catalyzed electrochemical etching mechanism was investigated via monitoring Au^{3+} concentration during etching, as well as the effects of etching time, metal film thickness, and wafer doping level. The transport characteristics of field-effect transistors based on individual SiMW revealed a typical *p*-type semiconducting behavior, with an on/off ratio as high as 10^3, a hole mobility of 32.7 $cm^2\ V^{-1}\ S^{-1}$ at $V_{ds} = -0.06$ V, and a hole concentration of $8.90 \times 10^{16}\ cm^{-3}$.

KEYWORDS: Silicon Microwires, Chemical Etching, Gold-Catalyzed, Field Effect Transistor.

1. INTRODUCTION

One-dimensional silicon nanowires (SiNWs) have attracted intense interest in recent years for their interesting semiconducting, mechanical, and optical properties, and promising applications in nanodevices.[1] SiNWs have been successfully used in field-effect transistors (FETs),[2] bio- and chemo-sensors,[3–5] integrated logic circuits,[6] solar cells,[7] lithium-ion battery anodes,[8, 9] and *p–n* junctions.[10] Various methods have been used to fabricate SiNWs, such as vapor–liquid–solid (VLS) growth,[11, 12] oxide-assisted growth (OAG),[13] and solid-liquid-solid (SLS),[14] SiNWs thus obtained are typically randomly oriented, and difficult for device applications. Therefore, achieving precise control of crystallographic orientation, dimension, and doping level of silicon nanostructures remains a challenging issue for device applications.

Homogeneous silicon micro/nanowires (SiMWs and SiNWs) arrays with identical dimensions, uniform surface state, and internal properties are typically needed as building blocks for electronic devices. As a typical bottom-up approach, vapor–liquid–solid (VLS) growth method is a feasible way for synthesis of SiNWs arrays with controlled wire diameter and density.[15, 16] Large-area SiMWs arrays have been synthesized via the VLS growth using a patterned buffer layer.[17] Ordered single-crystal SiNWs arrays have been synthesized by Au-assisted pyrolysis of silane inside nanochannel alumina (AAO) templates.[18] While the diameter of Si micro/nanowires can be somewhat controlled, uniform and controlled doping in Si wires is difficult and remains a challenge. The alternative, top-down approach using plasma etching is widely used in Si processing because of its advantages of high-resolution, high throughput and automation.[19, 20]

Recently, metal-assisted wet etching for the preparation of SiNWs arrays has attracted wide interest due to its salient advantages such as simplicity, easiness, control, etc.[21–23] The metal-assisted etching approach has been used to synthesize 2-dimensional (2D) periodic arrays of SiNWs via patterned metal film.[24, 25] Utilizing AAO as a pattern mask, spatially well-separated SiNWs arrays with diameters of <10 nm were fabricated.[26] In addition, uniform SiNWs arrays were grown by combining interference lithography (IL) and metal-induced etching.[27] In this paper, we report a new wet etching method, which can produce well-patterned SiMWs arrays with tunable wire diameters,

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lengths and growth orientations. Transport characteristics of FETs constructed from individual silicon submicrowires (SiSMWs) were systematically investigated.

2. EXPERIMENTAL DETAILS

In this work, seven types of Si wafers were used: *n*-type (100) wafers with a resistivity of 5–12, 0.48–0.66, and 0.00005–0.0001 Ω cm, *n*-type (110), (111) and (113) wafers of 5–12 Ω cm, and *p*-type (100) Si wafers of 5–12 Ω cm. All wafers were cut to pieces of 1×1 cm^2, and the wafer surfaces were conditioned hydrophilic by washing at room temperature with water for 10 min, and acetone for 6 min, followed by immersion in a hot Piranha solution (H_2SO_4/H_2O_2 4:1 (v/v)). The synthetic process of SiMWs arrays is schematically exhibited in Figure 1. First, an AZ5206E photoresist film of 300–500 nm thick was spin-coated (2500 r/m, 35 s) on a clean Si wafer. The wafer was next baked at 95 °C for 12 min followed by UV exposure with a contact mask. The photoresist was treated with a developer (MIF-300), leaving well-patterned circular-shaped photoresist dots on the Si wafer. Over-development of the photoresist up to 5 minutes was used to fine tune the diameter of the resulting Si wires. Secondly, an Au film of 40 nm was deposited onto the patterned Si substrate. Thirdly, the photoresist dots and the gold film on top of them were removed via ultrasonication in an acetone bath, leaving the silicon surface covered with a gold film with voids in where the photoresist dots originally were. Finally, the sample was immersed into an aqueous solution of HF and H_2O_2 for etching. In all etching experiments the concentrations of the HF and H_2O_2, unless otherwise specified, were 4.4 and 0.46 M, respectively. The etching was carried out in the dark for different durations.

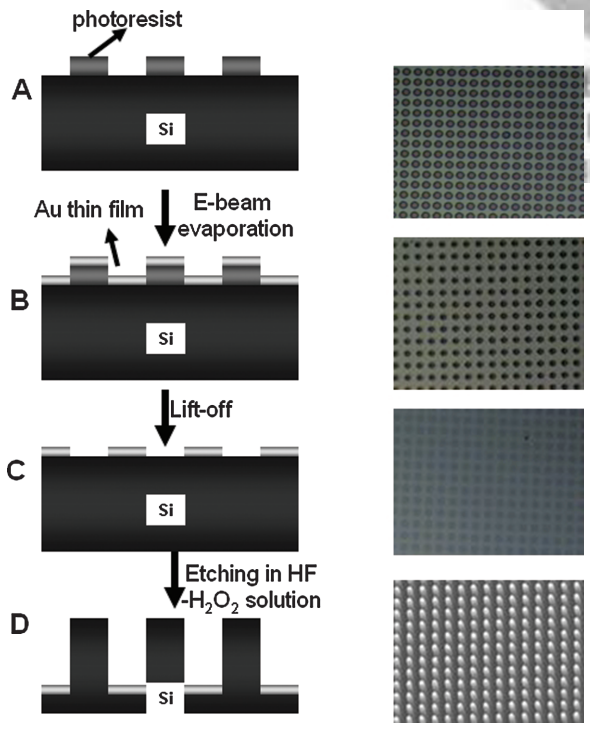

Fig. 1. Schematic illustration of the fabrication procedures and the corresponding morphology at different stages.

The morphology, crystal structure and composition of the products were characterized using scanning electron microscopy (SEM Philips XL 30 FEG) and high-resolution transmission electron microscopy (HRTEM, CM200 FEG operated at 200 kV). Au^{3+} concentrations were monitored with an optical emission spectrometer (Optima, 2100DC, PerkinElmer, USA). Electrical measurements were carried out on a semiconductor characterization system (4200-SCS, from Keithley Company) with pA sensitivity.

3. RESULTS AND DISCUSSION

3.1. Morphology and Structural Analysis of SiMWs

Figure 2 shows the representative SEM images of the SiMWs arrays obtained from different etching times. Figure 2(a) shows the (100) silicon substrate after 2 minutes etching, revealing all microwires are uniform with 2 μm diameter and 3 μm inter-wire spacing. The cross-section SEM images of the SiMWs arrays from different etching times are shown in Figure 2(b) (8 min), 2(c) (20 min), 2(d) (50 min), and 2(e) (100 min), revealing the wire length of 5, 15, 40, and 55 μm, respectively. Figure 2(f) shows that in the first 20 min of etching the etching depth (or the length of SiMWs) increased linearly with etching time, in agreement with previous report,[9] at an etching rate of 1 μm/min, which is comparable to that obtained by using silver catalyst.[28] However, after about 20-minute etching, the rate decreased to 0.5 μm/min.

When the etching duration was continued to 4 hours, many SiMWs fell down and the wire diameters reduced to 1 μm from the original 2 μm, as shown in Figure 3. Figure 3(b) shows increasing etching duration causes collapse of more SiMWs, and by 8 hours, i.e., Figure 3(c), almost all wires collapsed and became randomly oriented. Finally, at 12 h etching (Fig. 3(d)), all SiMWs collapsed with many voids and dimples formed in the wire bodies.

In the present etching approach, the diameters of SiMWs are primarily dictated by the dimension of the metal film, which is in turn determined by the photoresist dots pattern. To achieve size control of the wires, the size of the photoresist pattern was changed by over-developing the photoresist. The exposed AZ5206E positive photoresist could easily dissolve in the AZMIF-300 solution within 50 s, while dissolution of unexposed photoresist would take much longer time. In this work, the pattern was 2.5 μm in diameter and the resolution for the mask aligner was 1 μm. Consequently, the UV exposure at the edge of the

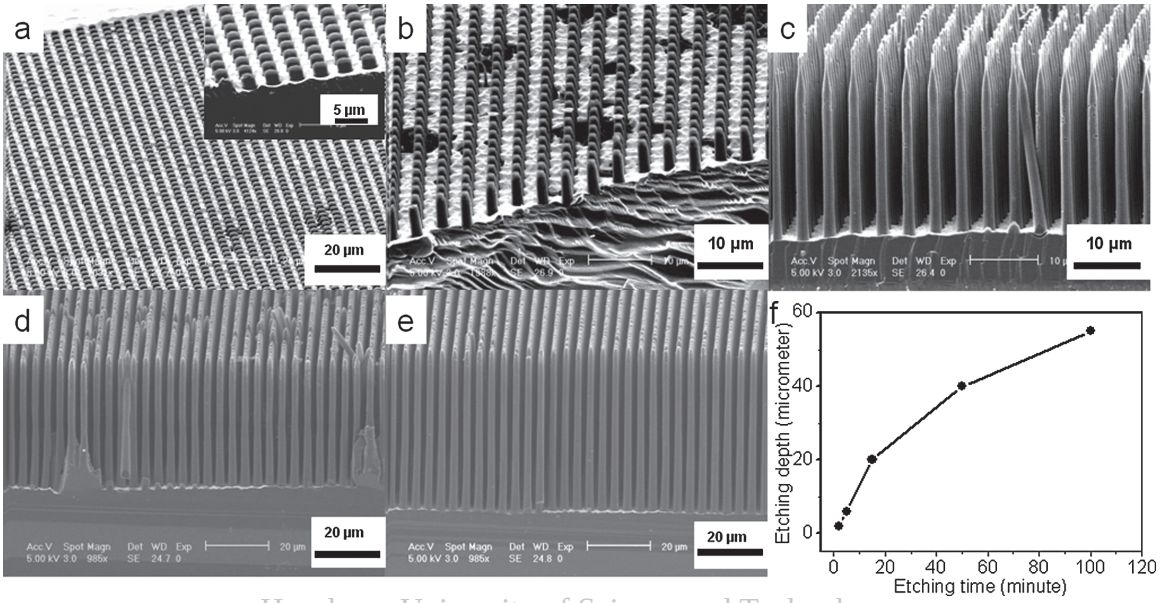

Fig. 2. SEM images of as-prepared SiMWs arrays obtained after different etching time. (a) 2 min, inset is a magnified image. (b) 8 min. (c) 20 min. (d) 50 min. and (e) 100 min. (f) Etching length of SiMWs versus etching time.

pattern would not be an ideal step function. The transition from the unexposed to the exposed region would extend over a micrometer. Considering the gradual change in UV-exposure near the edge region, the diameter of the ring-like photoresist dots pattern thus can be precisely controlled by over-developing for durations from 0 to 5 min. Figure 4 shows the as-prepared uniform silicon wires, whose diameters were controlled by overdeveloping duration. The wire diameters are 2.5, 2.0, 1.5, 1.0, and 0.6 μm for over-developing time of 0, 0.8, 1.7, 2.9, and 5.0 min, respectively. The relationship between the over-developing time and the wire diameters is shown in Figure 4(f).

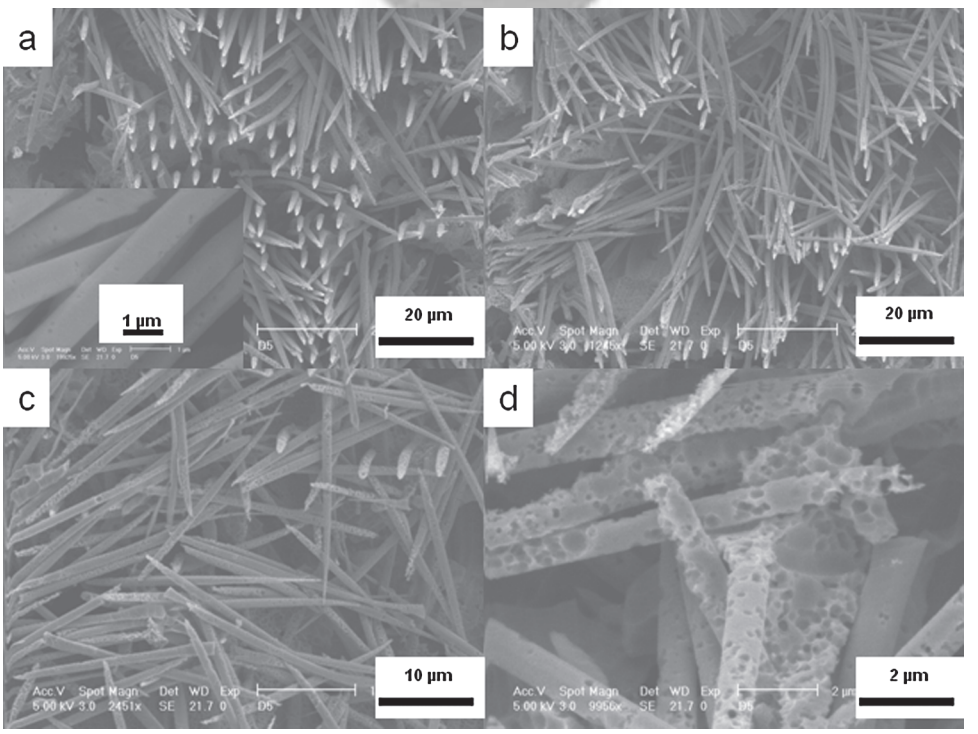

Fig. 3. SEM images of SiNWs etched in HF and H_2O_2 for different times: (a) 4 hours. Inset is a magnified SEM image of SiMWs; (b) 6 hours; (c) 8 hours; and (d) 12 hours.

Since the fabricated Si wires were too thick to allow electron penetration, the wires were reduced in diameter by oxidation and HF etching before TEM characterization. Figure 5(a) shows a typical TEM image of a SiMW after thinning down to a diameter of 200 nm. The energy-dispersive X-ray spectrum (EDX, Fig. 5(b)) shows only a single Si peak. High-resolution TEM image combined with SAED (Figs. 5(c and d)) shows the direction of silicon wire is along [100] direction.

3.2. Etching Mechanism

For silver-assisted silicon etching, the process is normally electrochemical in nature.[29] That is, silicon loses electrons to form Si ion, while H_2O_2 accepts electrons to form O_2. The electrochemical reaction is catalyzed by silver particles, producing anisotropic Si etching.[30] Here, we propose a similar mechanism to account for the Au-assisted etching process to form SiMWs, as shown in Figure 6.

The reaction process can be considered in two stages. The first stage is a vertical etching process (from 0 to 2 h), which primarily digs into the Si wafer, while the second is a lateral etching process (starting from 2 hour), which primarily etches the preformed Si columns. During the first stage or vertical etching process, the surface gold atoms in the deposited film is oxidized spontaneously to Au^{3+} ions in the presence of HF–H_2O_2, since the standard potential difference ($\Delta_r E_3^0$) of the two half cell reactions (1) and (2) is larger than zero at +0.356 V.[31] The overall chemical reaction can be formulated as in Eq. (3);

$$2H_2O_2(aq) + 4H^+(aq) + 4e^- \rightarrow 2H_2O + O_2(g) \qquad E^0(H_2O_2/O_2) = +1.776\ \text{V} \tag{1}$$

$$Au \rightarrow Au^{3+}(aq) + 3e^- \qquad E^0(Au/Au^{3+}) = -1.42\ \text{V} \tag{2}$$

$$6H_2O_2 + 12H^+ + 4Au \rightarrow 4Au^{3+} + 6H_2O + 3O_2 \qquad \Delta_r E_3^0 = +0.356\ \text{V} \tag{3}$$

Formation of Au^{3+} was indeed confirmed by analysis of the etching solution. Figure 7 shows the optical emission intensity of Au^{3+} ion versus the etching time. It reveals that in the initial 0–10 min Au^{3+} concentration increased sharply from 0 to 1.8×10^{-7} M. Significantly, once Au^{3+} ion concentration reached the maximum, it started to slowly decrease after ca. 120 minute of etching.

After the formation of Au^{3+} ions, silicon atoms in the vicinity of the Au^{3+} ions will be oxidized to Si^{4+} forming SiF_6^{2-}; this redox reaction can be represented as Eq. (6).

$$Si + 6F^-(aq) \rightarrow SiF_6^{2-}(aq) + 4e \qquad E^0(Si/Si^{4+}) = +1.24\ \text{V} \tag{4}$$

$$Au^{3+}(aq) + 3e^- \rightarrow Au \quad E^0(Au^{3+}/Au) = +1.42\ \text{V} \tag{5}$$

$$4Au^{3+}(aq) + 3Si(s) + 18F^-(aq) \rightarrow 4Au(s) + 3SiF_6^{2-}(aq) \qquad \Delta_r E_6^0 = 3.52\ \text{V} \tag{6}$$

Such a reaction (6) is kinetically feasible because $\Delta_r E_6^0$, the overall cell potential, is estimated at 2.665 V from $\Delta_r E_6^0 = (E_5 + E_4) - RT\ln[(SiF_6^{2-})^3/(Au^{3+})^4(F^-)^{18}]/nF$, where R is the gas constant, n the number of electrons participating in the half-cell reactions, F the Faraday constant, and (SiF_6^{2-}), (Au^{3+}), and (F^-) the concentration of SiF_6^{2-}, Au^{3+}, and F^-, respectively. (Au^{3+}) is approximately

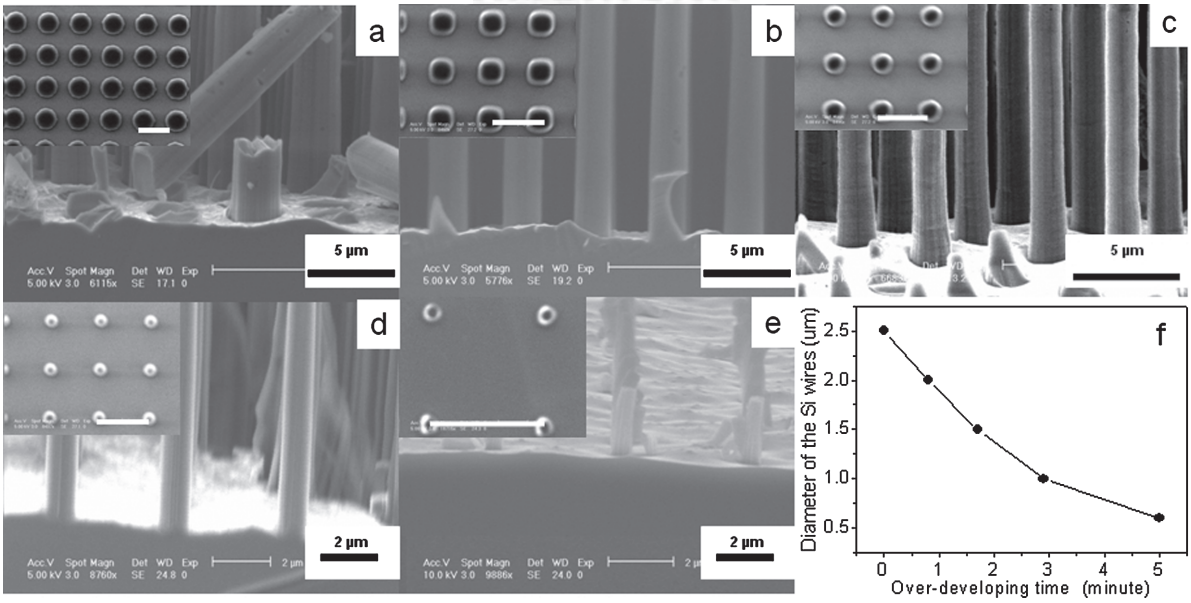

Fig. 4. Cross-section SEM images of SiMWs with different diameters: (a) 2.5 μm. (b) 2.0 μm. (c) 1.5 μm. (d) 1.0 μm. (e) 0.6 μm. Insets in (a–e) are the SEM images of the corresponding photoresist patterns dots. All the scale bars are 5 μm. (f) Over-developing time versus SiMWs diameter.

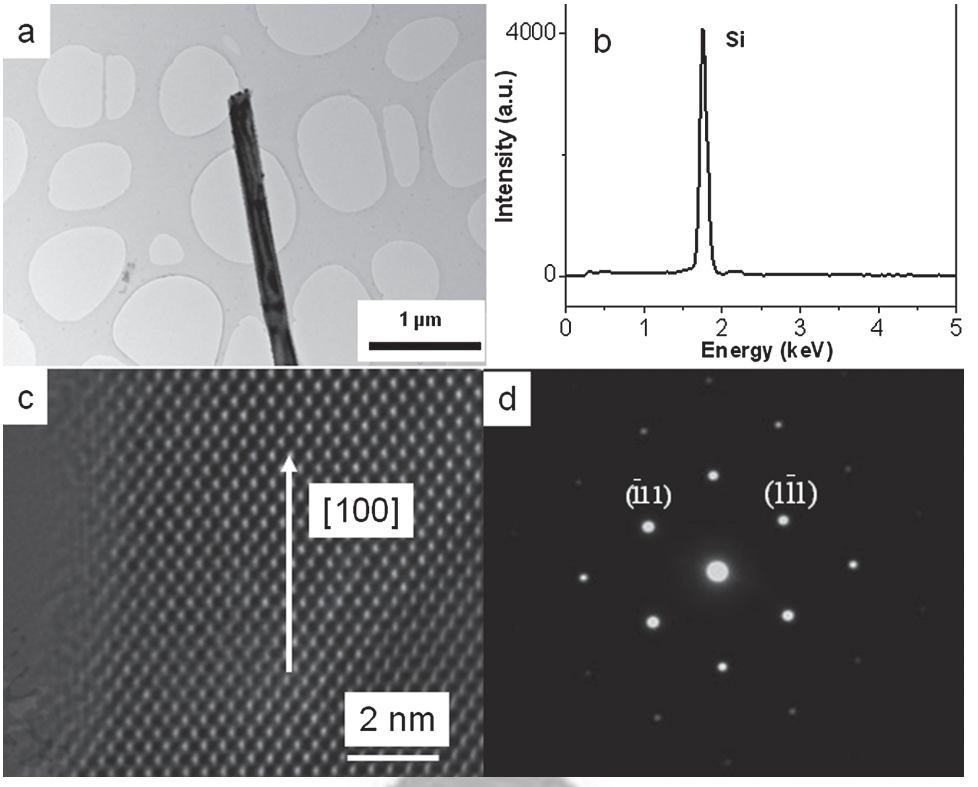

Fig. 5. (a) A TEM image of a typical silicon microwire after thinning down. (b) Corresponding EDX spectrum. (c) A HRTEM image and (d) the corresponding SAED pattern of the SiNW.

to 1.8×10^{-7} M according to the optical emission analysis, (F^-) is ca. 4.8 M considering the majority of HF remains in the etching solution, and (SiF_6^{2-}) is ca. 0.001 M as estimated from the weight loss from the reacted Si wafer. A close examination of the above results reveals a critical feature of the etching system; that is, in the etching process from 10 to 120 min, the quantity of gold atoms remains nearly constant. That is to say, Au serves effectively as a catalyst with its quantity in the mixed solution remaining almost constant during the vertical etching process. Indeed, this feature was confirmed by the optical emission analysis of the etching solution shown in Figure 7. Based on the above analysis, the overall reaction for Si etching can be represented as (7),

$$6H_2O_2(aq) + 12H^+(aq) + 3Si(s) + 18F^-(aq) \rightarrow 6H_2O + 3SiF_6^{2-}(aq) + 3O_2 \quad (7)$$

During the vertical etching process, the gold film works as a shield tunneling machine, while the Au^{3+} cations serve as the cutter of the machine. Au^{3+} cations continue to dig up the underneath Si atoms by oxidizing them to

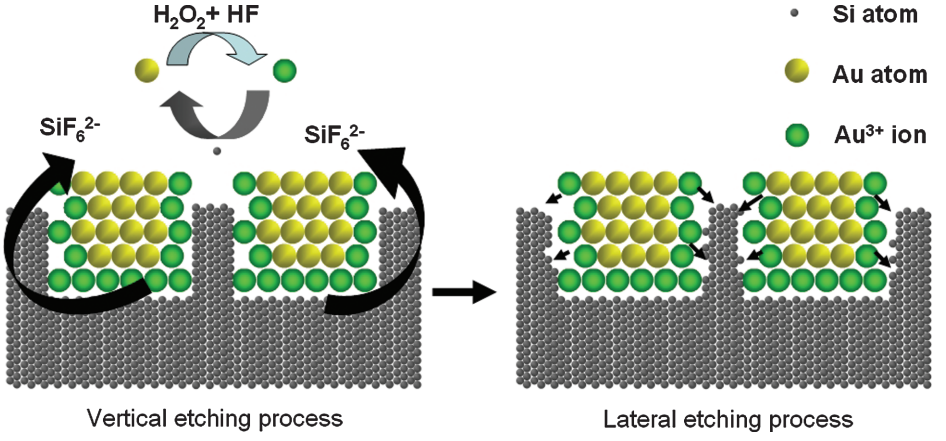

Fig. 6. Schematic illustration of the etching mechanism.

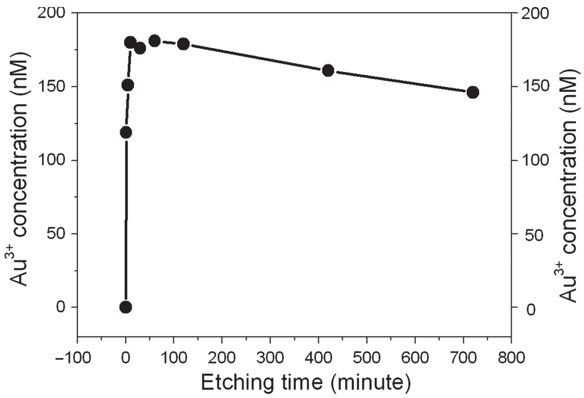

Fig. 7. Optical emission analysis of Au^{3+} concentrations at different etching times.

form soluble SiF_6^{2-} anions, concurrently the Au^{3+} cations are reduced to Au atoms. Such a digging process would last for about two hours, after which the Au^{3+} concentration began to decrease. At this stage, due to fast exhaustion of H_2O_2 and HF at the bottom of the gold film, a concentration gradient of H_2O_2 and HF is established, which decreases from the top to bottom. Consequently, the top part of the silicon columns was also etched by H_2O_2 and HF, leading to over-etching at SiMWs' tips, as can be seen in Figure 2(c). Obviously, this etching would not affect the growth direction of SiMWs.

As the etching process continued, the concentration of Au^{3+} dropped slowly from 1.8×10^{-7} M at 2 hours to 1.5×10^{-7} M at 12 hours (cf. Fig. 7), implying that the majority of H_2O_2 was gradually exhausted. Clearly, the previously observed shrinking of silicon microwires is due to depletion of H_2O_2 and insufficient Au^{3+} to maintain isotropic etching. At this stage we call it a lateral etching process, because then etching would not contribute to the lengthening of SiMWs. Instead, from here on the etching solution would begin to etch the SiMWs already formed.

Based on the above model, the observed decrease in etching or growth rate is understandable: The etching rate is decided by the concentrations of both Au^{3+} ions and HF. While Au^{3+} concentration was nearly the same throughout the vertical etching period (from 0 to 2 h), HF concentration would continue to decrease throughout the process. So, in the early stage at ca. 10 min of etching the growth rate is high, because the HF concentration is at maximum. As the etching proceeds, HF would be gradually consumed, thus the etching rate slowed down.

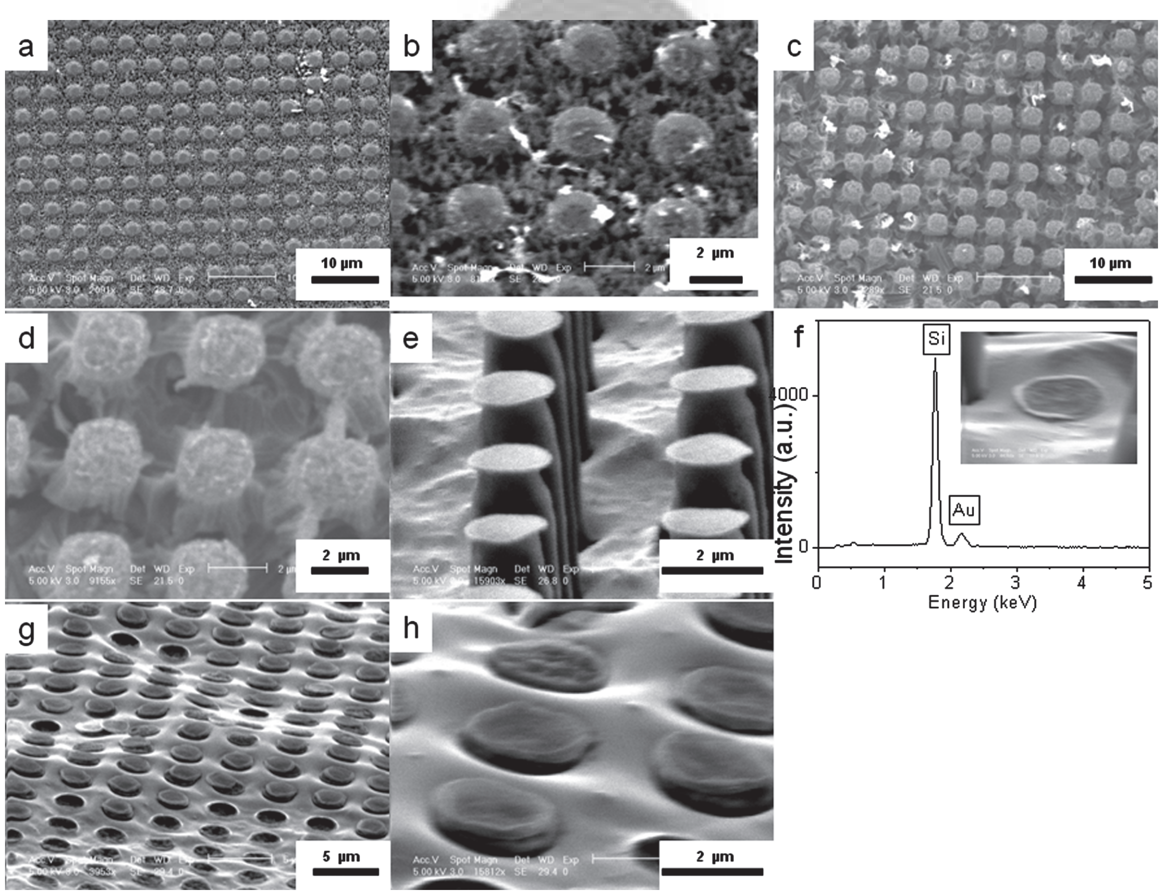

Fig. 8. SEM images of the product from gold film of different thickness; (a and b) 10 nm; (c and d) 20 nm; (e) 60 nm. (f) EDX analysis of the cap. Inset is a cap removed from the tip of the SiMW via ultrasonication. (g and h) are the SEM images of the product from 100 nm gold film at two magnifications.

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3.3. Factors Affecting the Etching Process

Beside etchant concentration and temperature, we now investigate how other factors may affect the formation of SiMWs arrays to probe the etching mechanism. In the etching process, the thickness of the gold film was found to play an important role in determining the morphology of SiMWs. As shown in Figures 8(a and b), when a silicon substrate with a pattern of 10 nm-thick gold film was immersed in the mixed solution of H_2O_2 and HF for 30 min, the wafer was etched to a depth of less than 1 μm. Close observation of Figure 8(b) reveals that removal of the surrounding surface of the silicon column is incomplete. As the Au film thickness was increased to 15 nm, the etching depth increased to several μm. At the same time, the surrounding surface of SiMWs was well-defined. Our experimental results showed the optimum thickness for etching is between 25–40 nm. Etching silicon wafer with a gold film thicker than this range would lead to the formation of a cap on each SiMWs, as shown in the inset of Figure 8(f). EDX analysis shows this cap to consist of silicon and gold. Since the microwire is pure silicon, the cap is considered to be pure gold. Note that etching silicon wafer with 100 nm thick patterned gold film produced no SiMWs. The flat surface and thinning of silicon wafer after etching is probably due to the fact that both vertical etching via gold and etching directly by H_2O_2 and HF happen at comparable rates.

Etching of *n*-type (100) silicon wafers with a resistivity of 0.48–0.66 Ω cm and 0.0005–0.001 Ω cm was compared to investigate the effect of doping level or wafer conductivity on the morphology of the final product. For convenience, all etching experiments were conducted for 30 min at room temperature, and the concentrations of both H_2O_2 and HF are identical to the previous condition. The results are shown in Figure 9, which reveals the etching depth is about 5 μm in the higher-resistivity wafer, and 1.5 μm in the lower-resistivity wafer. Noticeably, these etching depths are smaller than that in the wafer with a resistivity of 5–15 Ω cm. Further calculations show that the etching rates are 0.167 and 0.067 μm/min respectively for the wafer with a resistivity of 0.48–0.66 and 0.0005–0.001 Ω cm, which are also much smaller than that of the 5–15 Ω cm wafer. This observation is in sharp contrast to that observed when a mixed $HF/HNO_3/CH_3COOH$ solution was used as the etchant,[32] but is consistent with the result obtained using ethylenediamine-pyrocatechol-water mixed solution.[33] The detailed mechanisms for this resistivity-dependent etching behavior are unclear and require further study.

To investigate the effect of wafer orientation on etching behavior, (110), (111) and (113) oriented silicon wafers with nearly the same resistivity were etched under identical conditions. Figure 10(a) shows the cross-section SEM image of the (110) substrate after 30 min etching, which

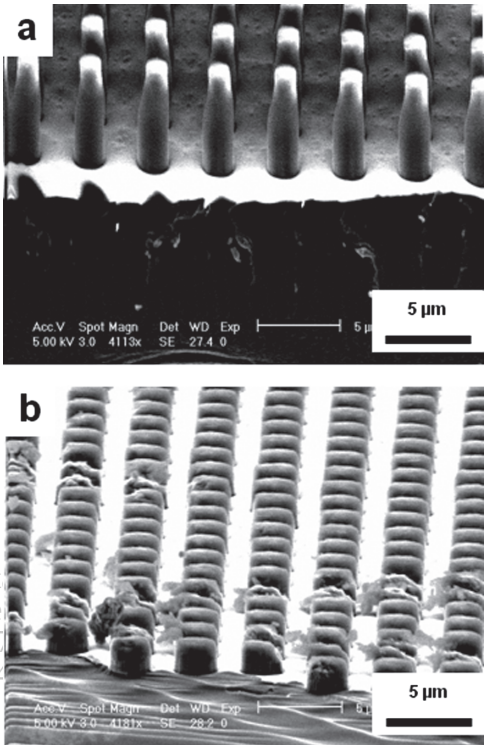

Fig. 9. Representative cross-sectional SEM images of SiMWs etched from wafers with different resistivity: a) 0.48–0.66 Ω cm. (b) 0.0005–0.001 Ω cm wafer.

reveals that all the microwires are uniform with approximately the same length and diameter. When the etched silicon wafer with microwires arrays were placed on a horizontal platform in SEM chamber, the top-view SEM image (inset of Fig. 10(a)) shows that all SiMWs are vertical to the Si wafer surface. This finding is in agreement with the previous result that metal sinking direction is normal to the Si surface.[34] Interestingly, similar alignments were also observed on (111) and (113) silicon wafers (see Figs. 10(b and c)). Obviously, the length directions of the SiMWs obtained from the above three wafers are [110], [111] and [113], respectively. This alignment manner of SiMWs is partially different from SiNWs etched using gold nanoparticles.[35] In the latter case, while the length direction of SiNWs etched from the (100) and (111) wafers are along [100] and [111] direction, respectively,[36] but the direction of SiNWs from (110) and (113) wafers are both along [100] direction. Such a discrepancy in etching directions due to the form of catalyst is unusual, and is quite diverse from the result observed on silver catalyzed silicon etch, in which, no matter of whatever form the catalyst in, the directions of SiNWs etched from (110), (113) oriented wafer are always along [100].[25] We think this distinction is probably due to the dominant role the gravity of the gold thin film played during solution etching. Although the detailed mechanism is still unclear, the isotropic character in Si etching by Au can be useful, because it will facil-

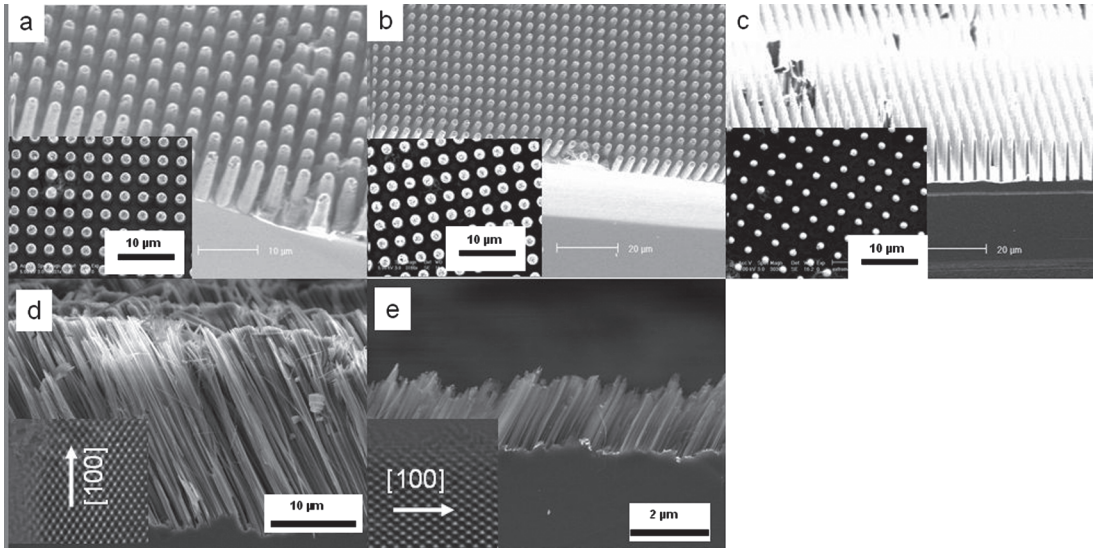

Fig. 10. SEM images of SiMWs and SiNWs with different length directions: (a) SiMWs arrays from (110) silicon wafer. (b) SiMWs arrays from (111) silicon wafer. (c) SiMWs arrays from (113) silicon wafer. The insets in (a–c) show the corresponding SEM images in the direction vertical to silicon wafer surface. (d) Cross-section SEM image of silicon etched from (110) Si wafer by using gold nanoparticles as catalysts. (e) Cross-section SEM image of silicon etched from (113) Si wafer by using gold nanoparticles as catalysts. The insets in (d and e) are the HRTEM images of the corresponding SiNWs.

itate the synthesis of SiMWs arrays with various growth directions.

3.4. FET Study of the Sub-Microwires

To explore the potential of Si sub-microwires (SiSMWs) for device application, SiSMW etched from a *p*-type (100) Si wafer with a resistivity of 5–12 Ωcm was used to construct FETs. In a typical process, the etched SiSMWs were scratched from the Si wafer, and dispersed in alcohol solution. The suspended SiSMWs were then transferred onto a SiO_2/Si substrate. Standard photolithography and metal film deposition were carried out to make the Ti/Au source and drain electrodes. Electrical measurements were performed in air at room temperature. Figure 11(a) show the typical characteristics of the as-prepared *p*-channel SiSMW-based FET. Based on a wire diameter of 0.6 μm and a channel length of 4 μm, the conductivity of the SiSMWs was calculated to be 2.1 S m^{-1}. The hole mobility (μ) was determined utilizing the following formula.

$$\mu_{\text{eff}} = \frac{dI_{\text{ds}}}{dV_g} \frac{\ln(4h/d)L}{2\pi\varepsilon_0\varepsilon_{\text{SiO}_2}V_{\text{ds}}}$$

Where h is the thickness of the SiO_2 dielectrics layer; d is the diameter of the SiSMW; L is length of the active microwire channel; $\varepsilon_{\text{SiO}_2}$ is the dielectric constant of the SiO_2 layer. From the left I_{ds}–V_g curve recorded at $V_{\text{ds}} = -0.06$ mV in Figure 10(b), a threshold voltage of 18 V can be deduced. Furthermore, dI_{ds}/dV_g can be calculated to be 1.23×10^{-8} S, in the linear regime from −6 to 12 V. Based on these values, the mobility is calculated to be 32.7 cm^2 V^{-1} s^{-1} at $V_{\text{ds}} = -0.06$ V; this value is comparable to that of SiNWs produced from similar chemical etching method,[37] but is remarkably lower than that of the mother wafer with a resistivity of 5–12 Ω cm, whose mobility is in the range 453–461 cm^2 V^{-1} s^{-1}.

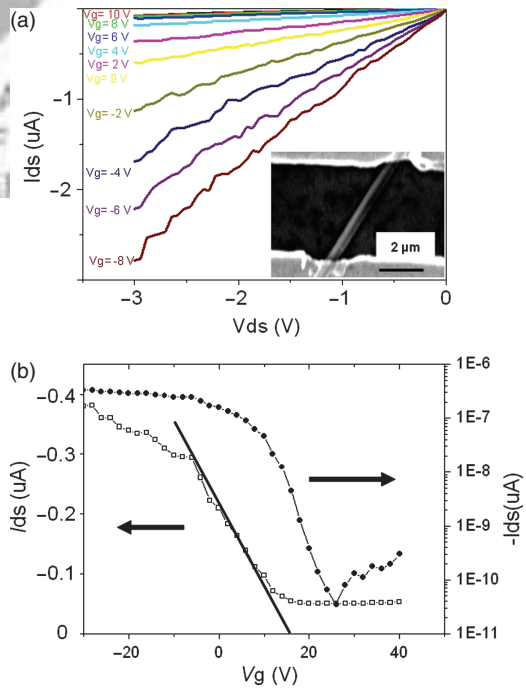

Fig. 11. Transistor characteristics of SiSMWs FET devices on SiO_2/Si substrate: (a) Typical I_{ds} versus V_{ds} curves under different V_g. Inset is the photograph of a typical FET device. (b) I_{ds}–V_g recorded at $V_{\text{ds}} = -0.06$ V, I_{ds} is shown in both linear and logarithmic plots.

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We attribute the reduced mobility to the scattering effect of rough surface.

The semi-logarithmic plot of I_{ds} versus V_g at a constant $V_{ds} = -0.06$ V in the right side of Figure 10(b) reveals an on-off current ratio (I_{on}/I_{off}) of the SiSMW FET larger than 10^3. Additionally, the hole concentration is calculated to be 8.90×10^{16} cm^{-3} using the equation of $\rho = 1/n_h q \mu_h$. Apparently, the hole concentration of the silicon microwires is larger than that of the p-type 5–12 Ω cm silicon wafer, which is less than 10^{16} cm^{-3}. In light of hydrogen termination of silicon wire surface, the observed enhancement in hole concentration is attributable to surface transfer doping.[37, 38]

4. CONCLUSIONS

We report a simple, metal-assisted chemical etching method for wafer-scale fabrication of single-crystal SiMWs with well-controlled diameters. This metal-assisted etching combined with photolithographic pre-patterning of silicon wafer can produce highly-ordered, patterned SiMWs with controlled directions. Transport characteristics of FET fabricated from individual SiSMW from a p-Si wafer revealed a typical p-type semiconducting behavior, with an on/off ratio $>10^{-3}$, a hole mobility of 32.7 cm^2 V^{-1} s^{-1} at $V_{ds} = -0.06$ V, and a hole concentration of 8.90×10^{16} cm^{-3}. These results illustrate the high potential of the as-prepared SiMWs for device applications.

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References and Notes

1. C. M. Lieber and Z. L. Wang, *MRS Bull.* 32, 99 (**2007**).
2. Y. Cui and C. M. Lieber, *Science* 291, 851 (**2001**).
3. Y. Cui, Q. Weir, H. Park, and C. M. Lieber, *Science* 293, 1289 (**2001**).
4. M. W. Shao, Y. Y. Shan, N. B. Wong, and S. T. Lee, *Adv. Funct. Mater.* 15, 1478 (**2005**).
5. L. B. Luo, J. S. Jie, W. F. Zhang, Z. B. He, J. X. Wang, G. D. Yuan, W. J. Zhang, L. C. M. Wu, and S. T. Lee, *Appl. Phys. Lett.* 94, 193101 (**2009**).
6. Y. Huang, X. F. Duan, Y. Cui, L. Lauhon, J. K. H. Kim, and C. M. Lieber, *Science* 294, 1313 (**2001**).
7. K. Q. Peng, X. Wang, and S. T. Lee, *Appl. Phys. Lett.* 16, 163103 (**2008**).
8. C. K. Chan, H. L. Peng, G. Liu, K. Mcllwrath, X. F. Zhang, R. A. Huggins, and Y. Cui, *Nat. Nanotechnol.* 1, 31 (**2008**).
9. K. Q. Peng, J. S. Jie, W. J. Zhang, and S. T. Lee, *Appl. Phys. Lett.* 93, 033105 (**2008**).
10. K. Q. Peng, Z. P. Huang, and J. Zhu, *Adv. Mater.* 16, 73 (**2004**).
11. Y. Y. Wu and P. D. Yang, *J. Am. Chem. Soc.* 123, 3165 (**2001**).
12. Y. Cui, L. J. Lauhon, M. S. Gudiksen, J. Wang, and C. M. Lieber, *Appl. Phys. Lett.* 78, 2214 (**2001**).
13. W. S. Shi, H. Y. Peng, Y. F. Zheng, F. N. Wang, N. G. Shang, Z. W. Pan, C. S. Lee, and S. T. Lee, *Adv. Mater.* 12, 1343 (**2000**).
14. H. F. Yan, Y. J. Xing, Q. L. Hang, D. P. Yu, Y. P. Wang, J. Xu, Z. H. Xie, and S. Q. Feng, *Chem. Phys. Lett.* 323, 224 (**2000**).
15. Y. Wang, V. Schmidt, S. Senz, and U. Gösele, *Nat. Nanotech.* 1, 186 (**2006**).
16. W. K. Choi, T. H. Liew, H. G. Chew, F. Zheng, C. V. Thompson, Y. Wang, M. H. Hong, X. D. Wang, L. Li, and J. Yun, *Small* 4, 330 (**2008**).
17. K. E. Plass, M. A. Filler, J. M. Spurgeon, B. M. Kayes, S. Maldonado, B. S. Brunschwig, H. A. Atwater, and N. S. Lewis, *Adv. Mater.* 20, 1 (**2008**).
18. X. Y. Zhang, L. D. Zhang, G. W. Meng, G. H. Li, P. Y. Jin, and F. Phillipp, *Adv. Mater.* 13, 1238 (**2001**).
19. B. K. Teo and X. H. Sun, *Chem. Rev.* 107, 1454 (**2007**).
20. S. A. Campbell, The Science and Engineering of Microelectronic Fabrication, Second Edition, Oxford University Press, New York (**2001**).
21. W. A. Kern and C. A. Deckert, Chemical Etching: in Thin Film Processing, Academic, New York (**1978**).
22. K. Q. Peng, Y. J. Yao, S. P. Gao, and J. Zhu, *Adv. Mater.* 14, 1164 (**2002**).
23. K. Q. Peng, H. Fang, J. J. Hu, Y. Wu, J. Zhu, Y. J. Yan, and S. T. Lee, *Chem. Eur. J.* 12, 7942 (**2006**).
24. Z. P. Huang, H. Fang, and J. Zhu, *Adv. Mater.* 19, 744 (**2007**).
25. K. Q. Peng, M. L. Zhang, A. J. Lu, N. B. Wong, R. Q. Zhang, and S. T. Lee, *Appl. Phys. Lett.* 90, 163123 (**2007**).
26. Z. P. Huang, X. X. Zhang, M. Reiche, L. F. Liu, W. Lee, T. Shimizu, S. Senz, and U. Gösele, *Nano lett.* 8, 3047 (**2002**).
27. W. K. Choi, T. H. Liew, M. K. Dawood, H. I. Smith, C. V. Thompson, and M. H. Hong, *Nano. Lett.* 11, 3799 (**2008**).
28. C. Y. Chen, C. S. Wu, C. J. Chou, and T. J. Yen, *Adv. Mater.* 20, 3811 (**2008**).
29. K. Q. Peng, J. J. Hu, Y. J. Yan, Y. Wu, H. Fang, Y. Xu, S. T. Lee, and J. Zhu, *Adv. Funct. Mater.* 16, 387 (**2006**).
30. M. L. Zhang, K. Q. Peng, X. Fan, J. S. Jie, R. Q. Zhang, S. T. Lee and N. B. Wong, *J. Phys. Chem. C* 112, 4444 (**2008**).
31. W. D. Callister, Jr, Materials Science and Engineering: An Introduction, John Wiley & Sons, Inc., US (**1997**).
32. H. Muraoka, Controlled Preferential Etching Technology, Electrochemical Society, Princeton, NJ (**1973**).
33. J. C. Greenwood, *J. Electrochem. Soc.* 116, 1325 (**1969**).
34. H. F. Fang, Y. Wu, J. H. Zhao, and J. Zhu, *Nanotechnology* 17, 3768 (**2006**).
35. K. Q. Peng, A. J. Lu, R. Q. Zhang, and S. T. Lee, *Adv. Funct. Mater.* 16, 3026 (**2008**).
36. K. Q. Peng, Y. Wu, H. Fang, X. Y. Zhong, Y. Xu, and J. Zhu, *Angew. Chem. Int. Ed.* 44, 2737 (**2005**).
37. J. S. Jie, W. J. Zhang, K. Q. Peng, G. D. Yuan, C. S. Lee, and S. T. Lee, *Adv. Funct. Mater.* 18, 3251 (**2008**).
38. C. S. Guo, L. B. Luo, G. D. Yuan, X. B. Yang, R. Q. Zhang, W. J. Zhang, and S. T. Lee, *Angew. Chem. Int. Ed.* 48, 9896 (**2009**).