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# High-performance CdS:P nanoribbon field-effect transistors constructed with high-κ dielectric and top-gate geometry

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High-performance field-effect transistors (FETs) based on single phosphorus-doped $n$-type CdS nanoribbon with high-κ HfO$_2$ dielectric and top-gate geometry were constructed. In contrast to the nano-FETs that were fabricated on SiO$_2$/Si substrate with back-gate device configuration, the top-gate FETs exhibit a substantial improvement in performances, i.e., work voltage was reduced to a small value of within $\pm 5$ V, the subthreshold swing was reduced to 200 mV/dec and the $I_{on}/I_{off}$ ratio was increased by about six orders of magnitude. The top-gate CdS:P nano-FET shows high sensitivity upon light irradiation, revealing that the top-gate FETs are promising candidates for nanoelectronic and optoelectronic applications. © 2010 American Institute of Physics.
[doi:10.1063/1.3360206]

One-dimensional group II-VI semiconductor nanostructures such as ZnS, CdS, and CdSe nanowires/nanoribbons (NRs) have attracted much attention in recent years owing to the unique optical and electrical properties derived from the quantum confinement effects and the large surface effects. They are promising building blocks for diverse device applications, including biosensors, energy conversion, nanoelectronics, and nanooptoelectronics.[1–3] As a fundamental unit in functional nanodevices, such as integrated circuits and display systems, the construction and integration of field-effect transistors (FETs) based on the semiconductor nanostructures have been intensively researched and great progresses have been achieved in the past decade.[2–4] However, nano-FETs in current researches usually have a basic device structures, in which low-κ SiO$_2$ ($\sim$3.9) and heavily doped Si substrate are served as dielectric and global back-gate electrode, respectively, resulting in a poor device performance and low capability for large scale integration.

Contact resistance caused by interface defects and the work function mismatch is usually observed in the semiconductor devices. Large contact resistance will result in the device performance degradation and is needed to be eliminated for realizing high-performance devices. To reduce the contact resistivity, besides the use of contact metal with appropriate work function, doping to the semiconductors has been demonstrated to be an efficient way. By doping, the Schottky barrier between nanostructures and electrodes becomes thinner and lower, allowing the carriers pass through the barrier easier. As a result, the series resistance is decreased and the work current of the FETs could be enhanced.[5–7] Further improvement of the device performance relies on the using of new dielectric materials as well as superior device structures.[8,9] For instance, by using the high-κ gate insulators, the gate can effectively modulate the channel conductance with relative thick dielectric film, thus decreasing the work voltage and meanwhile reducing the direct-tunneling leakage current.[5,9] On the other hand, optimization to the device configuration is also critical to realize high-performance devices. Top-gate and even surrounding-gate FETs are widely studied for achieving this aim.[10] The top-gate nano-FETs have many advantages over the conventional global back-gate devices, such as local gate biasing at low voltage, high speed switching, and high integration density.[11] Nevertheless, most of the efforts are devoted to carbon nanotubes (CNTs), oxide and III-V nanostructures so far, high-performance nano-FETs based on II-VI nanostructures remains a challenging issue.

Herein, we report the fabrication of top-gate nano-FETs with high-κ HfO$_2$ ($\sim$25) dielectric based on individual phosphorus-doped CdS NR. The CdS:P NR FETs shown excellent electronic and optoelectronic characteristics and have potential applications in nanoelectronics and optoelectronic devices.

To construct the top-gate nano-FETs from single CdS:P NR, the as-synthesized CdS NRs were uniformly dispersed on SiO$_2$ (300 nm)/p+Si (resistivity <0.02 Ω cm) substrate. The source and drain electrodes were defined by photolithography and subsequently In (80 nm) and Au (20 nm) deposition in a high-vacuum e-beam system. Afterwards, additional photolithography process was used to define the pattern for the top-dielectric layer. High-κ dielectric of HfO$_2$ (30 nm) layer was then deposited by atomic layer deposition (Cambridge Nanotech, Savannah-200) to serve as the gate insulator. Eventually, the Au (20 nm) top-gate electrodes were fabricated on the top of the HfO$_2$ dielectric layer via the photolithography and e-beam evaporation. Electrical measurements were carried out at room temperature by using a semiconductor characterization system (Keithley 4200).

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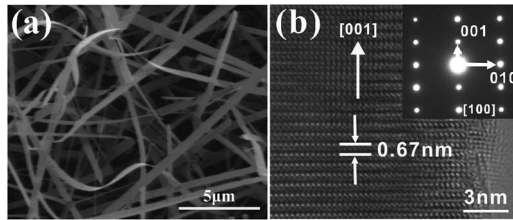b)Electronic mail: jsjie@hfut.edu.cn.

FIG. 1. (a) FESEM image of the as-synthesized CdS:P NRs. (b) HRTEM image and its corresponding SAED pattern of a typical CdS:P NR.

Figure 1(a) shows the SEM image of the as-synthesized CdS:P NRs, revealing that high-density brushy NRs were obtained in the substrates after 2 h growth. The CdS:P NRs have a uniform width of $0.5-1$ $\mu$m, a thickness of $\sim 30$ nm, and a typical length of $30-60$ $\mu$m. Moreover, HRTEM and the corresponding selected-area electron diffraction (SAED) pattern recorded along the [100] zone axis [Fig. 1(b) and its inset] indicate that the CdS:P NRs are hexagonal single crystals grown along the [001] orientation.

Schematic of the conventional back-gate nano-FET and the top-gate nano-FET are illustrated in Figs. 2(a) and 2(b), respectively. And Fig. 2(c) shows the SEM image of a typical top-gate nano-FET fabricated from an individual CdS:P NR with a channel length of 8 $\mu$m. To evaluate the effects of the dielectric materials and device configurations, both back- and top-gate devices are studied in this work for comparison. Figure 3(a) depicts the typical source-drain current ($I_{DS}$) versus bias voltage ($V_{DS}$) curves under varied gate voltages ($V_G$) from $-25$ to 5 V in a step of 5 V for a back-gate nano-FET. The linear curves reveal the good ohmic contact between the In electrodes and CdS:P NR. It is noted that the device exhibits the electrical characteristics of an $n$-channel FET. The $n$-type feature of the CdS NRs is most likely originated from the compensated donor defects such as S vacancies ($V_s$) and interstitial Cd atoms ($I_{Cd}$), which were induced by the high concentration P doping in CdS NRs. In contrast to the devices fabricated from CdS:P NRs, the devices based on intrinsic CdS NRs have very low conduction current ($<10^{-12}$ A) and almost no response to the gate voltage (figure not shown), indicating that doping is an efficient route to improve the device performance and which is particularly important for semiconductor nanostructures with low conductivity. Although the back-gate nano-FETs have shown obvious gating effect, the device performance is still too poor for practical applications: the work voltage of the device is



FIG. 3. (Color online) Electrical transfer characteristics of the back-gate FETs (a) $I_{DS}-V_{DS}$ curves of the back-gate CdS NR FET measured at varied $V_G$ from $-25$ to 5 V in a step of +5 V. (b) $I_{DS}-V_G$ curve at $V_{DS}=1$ V for the back-gate FET.

rather high ($>25$ V). Also a small $I_{on}/I_{off}$ ratio of $\sim 10$ and a low transconductance ($g_m$) of $\sim 7.3$ nS at $V_{DS}=1$ V can be deduced from Fig. 3(b). It is noted that the device cannot be fully depleted even at a large negative $V_G$ of $-25$ V and the ON current for this device is smaller than 0.2 $\mu$A ($V_G$ $=10$ V, $V_{DS}=1$ V). In addition, the electron mobility $\mu_n$ is estimated according to the equation, $g_m=dI_{DS}/dV_G$ $=(Z/L)\mu_n C_0 V_{DS}$ in the linear regime of $I_{DS}-V_G$ curve, where $Z/L$ is the width-to-length ratio of the channel. The capacitance per unit area is given by $C_0=\varepsilon\varepsilon_0/h$, where $\varepsilon$ is the dielectric constant (3.9 for $SiO_2$) and $h$ is the thickness of the $SiO_2$ dielectric layer. Based on the above equations, $\mu_n$ $\approx 14.8$ cm$^2$/V s is deduced. The threshold voltage ($V_{th}$) of the device is roughly estimated to be about $-14.3$ V from the linear part of the $I_{DS}-V_G$ curve. On the other hand, subthreshold swing ($S$), which represents the increase rate of $I_{DS}-V_G$ curve and a small $S$ is desired for high-speed switch, is an important parameter for an FET and this value can be determined by $S=\ln(10)[dV_G/d\ln I_{DS}]$. However, it is noted that the back-gate device in Fig. 3 shows very poor subthreshold characters and there is no obvious decline for $I_{DS}$ in the subthreshold region, which leads to a large $S$ of $>25$ V/dec.

Figures 4(a) and 4(b) depict the typical electrical transfer characteristics of the Au top-gate device, which show a remarkable improvement on the device performance as com-
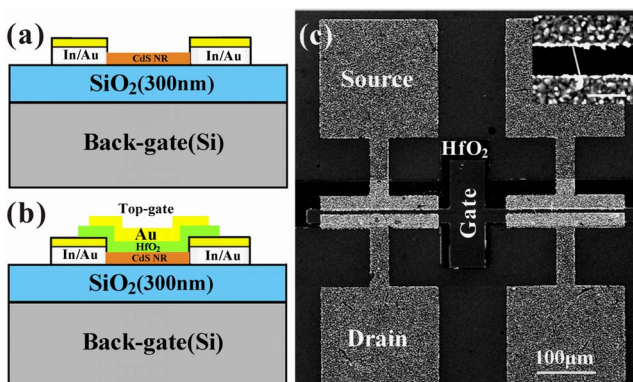


FIG. 2. (Color online) Schematic illustration of the back-gate (a) and the top-gate (b) CdS NRs FET. (c) SEM image of a representative top-gate device. The inset shows the enlarged SEM image of the FET channel.
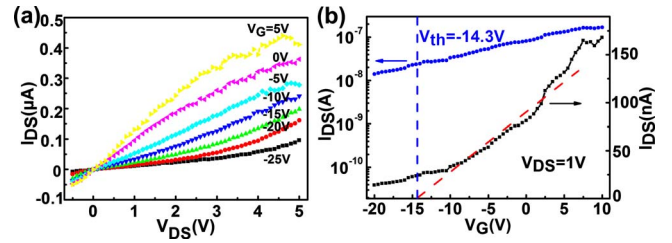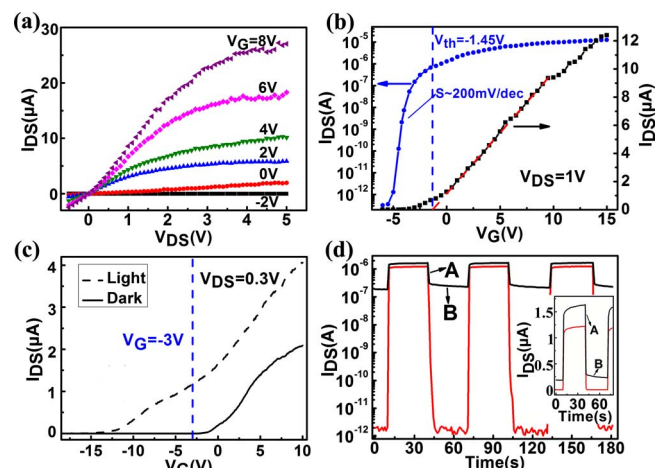


FIG. 4. (Color online) Electrical and photoelectrical characteristics of a typical top-gate CdS NR FET. (a) $I_{DS}-V_{DS}$ curves of the FET measured with varied gate voltages from $-2$ to 8 V in a step of +2 V. (b) $I_{DS}-V_G$ curve at $V_{DS}=1$ V. (c) $I_{DS}-V_G$ curves measured in dark (solid line) and in light irradiation (dashed line), respectively, at $V_{DS}=0.3$ V. (d) Time response of the CdS:P top-gate FET to the pulsed incident white light measured at $V_G$ $=-3$ V and $V_G=0$ V at $V_{DS}=0.3$ V. The linear scale view of the curve is shown in the inset.

pared with the back-gate device; working voltage for the top-gate device has decreased to a small range of $\pm 5$ V. From the transfer characteristics ($I_{DS}-V_G$) [Fig. 4(b)], it can be deduced that $V_{th}$ is about $-1.45$ V, $I_{on}/I_{off}$ ratio is larger than $10^7$, and the transconductance value $g_m$ is $\sim 0.87$ $\mu$S at $V_{DS}=1$ V, leading to a mobility value of 27.4 cm$^2$/V s. ON current for the top-gate device has increased to $\sim 10$ $\mu$A ($V_G=10$ V, $V_{DS}=1$ V). Significantly, the value of $S$ has dramatically decreases to $\sim 200$ mV/dec. Although this value is still larger than the theoretical minimum value of 60 mV/dec for MOSFET, it is comparable to some of the best results reported for CNT, Si, and ZnO nano-FETs.[12–14]

From the above measurements, it is shown that the use of high-$\kappa$ dielectric and top-gate geometry has led to a substantial improvement in the device performances for CdS:P NR FETs. The $I_{on}/I_{off}$ ratio and the transconductance for the top-gate nano-FETs have been enhanced by approximately $10^6$ and $10^2$ times, respectively, as compared with the back-gate CdS:P NR FETs. Meanwhile, the work voltage has decreased at least five times and the ON current has increased about 50 times. As we known, low work voltage is much desired for the electrical devices to reduce the energy consumption. The advantages of high-$\kappa$ dielectric in improving the device performances are evident, which affords high capacitance without relying on ultrasmall film thickness, leading to the large ON current, high ON/OFF ratio, small work voltage, and subthreshold swing value. On the other hand, in the top-gate nano-FETs, the conduction channel is fully encapsulated by the dielectrics (bottom by SiO$_2$, top by HfO$_2$ in our case) and the gate coverage to be channel is higher, thus allowing stronger charge coupling between the gate and the channel, which also contribute to the performance improvement.

CdS is a promising material for visible light detection due to its primary band gap of 2.4 eV and high sensitivity.[15] The light response of the top-gate FET is depicted in Figs. 4(c) and 4(d), which were recorded on the same device in Figs. 4(a) and 4(b). White light for microscope illumination served as the light source. From the transfer characteristics measured in dark (solid line) and in white light illumination (dashed line), respectively, it is seen that the $V_{th}$ has shifted dramatically from $-1.45$ to $-11$ V due to the increased carrier concentration in the NR upon light irradiation. The increased carrier concentration is attributed to the electron-hole pairs that excited by incident phonons with energy larger than the bandgap of CdS.[15] By fixing the $V_G$ at an appropriate value ($V_G=-3$ V is selected here), a high response ratio of $I_{light}/I_{dark}=10^6$ is obtained, in contrast to the small value of $\sim 10$ when no gate voltage ($V_G=0$ V) is applied. Moreover, due to existing of a negative gate voltage, the accumulated carrier could be depleted as soon as the incident light is turned off, leading to a fast photoresponse and the fall time is $<5$ s for the top-gate FET [Fig. 4(d)]. Moreover, the CdS:P NR photodetector also exhibits excellent stability and reproducibility. In contrast, when no $V_G$ is applied, the fall edge of the devices is composed of two following parts: a relative fast decay edge [marked by A in Fig. 4(d)] and a long decay tail (marked by B). The total fall time then increases to tens of seconds, which is obviously larger than the value of that when negative $V_G$ is applied. We note that the fall time for

the top-gate FETs at negative $V_G$ is larger than the previous report on the photodetectors based on the intrinsic CdS nanoribbons ($<1$ ms), whereas the response ratio is increased by about two orders of magnitude ($10^6$ versus $10^4$).[15] The higher concentration of defects and impurities in the P-doped CdS NRs is likely responsible for the lower response speed. The increased response ratio could be explained in terms of low contact resistance and higher sensitivity of the doped CdS NR to light.

In conclusion, high-performance nano-FETs based on individual NRs were constructed by using high-$\kappa$ HfO$_2$ dielectric and top-gate geometry. In contrast to the conventional back-gate nano-FET, the work voltage for the top-gate nano-FET was reduced from larger than $\pm 25$ V to a much smaller range of $\pm 5$ V, the subthreshold swing was decreased from $>25$ V/dec to 200 mV/dec, the transconductance was enhanced from 7.3 nS to 0.87 $\mu$S, and the $I_{on}/I_{off}$ ratio remarkably increased from $\sim 10$ to $\sim 10^7$, respectively. Study on the photoresponse of the CdS:P top-gate FET reveals that the sensitivity and response speed could be dramatically improved by applying an appropriate negative gate voltage. The high-performance CdS:P NR FETs may have great potential in nanoelectronic and optoelectronic applications.

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