

Synthesis of Sb-Doped *p*-Type CdTe Nanowires and Their Application as High-Performance Nano-Schottky Barrier Diodes

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ABSTRACT

p-type CdTe nanowires (NWs) were successfully synthesized by employing Sb as the dopant via a simple thermal evaporation method. CdTe:Sb NWs had single crystal zinc blende structure with [211] growth orientation. Electrical measurements on the single NW revealed a substantial enhancement on the NW conductivity after doping, which could be further tuned in a wide range of 4 orders of magnitude by adjusting the doping level. Nano-Schottky barrier diodes (nanoSBDs) based on Al/CdTe:Sb NW junctions showed excellent diode characteristics with low turn on voltage of $\sim +1$ V, high rectification ratio of $>10^7$, small ideality factor of ~ 1.67 , and large breakdown voltage of -17.5 V. By replacing the hard SiO₂/Si substrates with PET substrates, flexible nanoSBDs were constructed, which kept the high device performance while also showed the good stability under strains. It is expected that the CdTe NWs with controlled transport properties will have important applications in the future nanoelectronics.

KEYWORDS: CdTe Nanowires, Sb Doping, Schottky Barrier Diodes, Flexible Devices.

1. INTRODUCTION

Recently, semiconductor nanostructures with high aspect ratio, such as nanowires (NWs), nanoribbons (NRs), nanotubes (NTs), and multi-branched structures, have attracted considerable attention because of the novel physical and chemical properties that appeared in nanoscale.^{1–7} Among the semiconductor nanostructures, II–VI group nanomaterials have gained special interest due to their unique electronic and optoelectronic properties.^{8,9} Cadmium telluride (CdTe) is an important II–VI semiconductor with a direct band-gap of 1.5 eV at room temperature. The appropriate band-gap of CdTe allows the efficient absorption of the sun light so that it has been widely used in solar cells.¹⁰ CdTe also shows the potential as high-performance photoelectric detectors and sensors.^{11,12} So far, various growth techniques, including vapor phase evaporation,¹³ solution-based chemical synthesis,^{14,15} self-assembly from CdTe nanoparticles,¹⁶ and template-directed electrodeposition,^{17–20} have been developed to obtain one-dimensional (1D) CdTe nanostructures. In spite

of these progresses, the methods to tune the electrical transport properties of the CdTe nanostructures are seldom studied and their applications in electronic and optoelectronic devices need to be further exploited.

Owing to the outstanding mechanical properties of 1D nanostructures, such as high strength, and extraordinary flexibility and resilience, they show the great potential in the fields of flexible and transparent electronics.¹⁷ A host of semiconductor nanostructures, such as carbon NTs,^{21–27} ZnO NWs,²⁸ and In₂O₃ NWs,²⁹ have been utilized to construct flexible and transparent nanodevices for next-generation displays and integrated devices. However, there are few reports concerned about the applications of CdTe nanostructures in this field.

Herein, we report the fabrication of CdTe NWs with controlled *p*-type doping by using the V group element of Sb as the dopant. The conductivities of the CdTe NWs were greatly enhanced upon Sb doping and could be tuned in a wide range of 4 orders of magnitude by adjusting the doping level. Nano-Schottky barrier diodes (NanoSBDs) based on Al/*p*-CdTe NWs junctions exhibited excellent device performances. Also, by displacing the hard substrate with PET substrate, the CdTe:Sb NWs showed rigid promising application in flexible nanoelectronics.

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2. EXPERIMENTAL DETAILS

2.1. Synthesis and Characterizations of the *p*-Type CdTe:Sb NWs

Synthesis of the *p*-type CdTe NWs was conducted in a horizontal tube furnace by using Sb as the dopant *via* a thermal co-evaporation method, as shown in Figure 1. CdTe powder (99.99%) and Sb powder (99.999%) were loaded into two separated alumina boats, respectively, and transferred to the center region of the tube furnace. Sb source was placed next to the CdTe source at the upstream direction. Si substrates, which were ultrasonically cleaned in acetone and alcohol, respectively, and coated with 10 nm Au catalyst, were placed at the downstream position with a distance of ~10 cm away from the CdTe source. After that, the system was evacuated to a base pressure of 5×10^{-3} Pa, and then backfilled with a constant H₂ (5% in Ar) gas flow of 30 SCCM to a pressure of ~250 Pa. The furnace was heated up to 650 °C in 40 min and maintained at this temperature for 60 min. After the system was cooled down to room temperature, the Si substrates were taken out of the furnace and a layer of black wool-like product was observed on their surface. In this work, three samples with varied doping level were synthesized and marked as sample 1, sample 2, and sample 3, corresponding to the different CdTe:Sb weight ratio of 10:1, 4:1, and 1:1, respectively, in the evaporation sources. Intrinsic CdTe NWs were also synthesized under the same conditions except the Sb was not used for comparison.

The morphologies, structures, and compositions of the CdTe:Sb NWs were characterized by field-emission scanning electron microscope (FESEM, SIRION 200 FEG), X-ray diffraction (XRD, Rigaku D/Max-rB), energy-dispersive X-ray spectroscopy (EDX, attached on the SEM), X-ray photoelectron spectroscopy (XPS, Thermo

ESCALAB250), and high-resolution transmission electron microscope (HRTEM, JEOL JEM-2010).

2.2. Device Construction and Analysis

To assess the electrical properties of the CdTe:Sb NWs, back-gate field-effect transistors (FETs) based on single NW were constructed. First, the as-synthesized CdTe:Sb NWs were dispersed on SiO₂ (300 nm)/*p*+-Si substrate, and then photolithography and subsequently lift-off process were utilized to define Cu (4 nm)/Au (50 nm) source and drain double-layer electrodes on the NWs. The degenerately doped Si substrate acted as the global back gate in the nanoFETs. To construct the nanoSBDs, Al (60 nm) Schottky contacts were fabricated by additional photolithography and lift-off processes. Flexible nanoSBDs were constructed by the same processes except PET substrates instead of the rigid SiO₂/Si substrates were used. All the electrical measurements were conducted at room temperature with a semiconductor characterization system (Keithley 4200-SCS).

3. RESULTS AND DISCUSSION

3.1. Characterizations of the *p*-Type CdTe:Sb NWs

Figure 2(a) shows the typical FESEM image of the as-synthesized CdTe:Sb NWs. It is seen that the CdTe:Sb NWs grow from the underlying large CdTe crystals, which might be formed at relative low temperature during the heating process. The NWs have a uniform geometry with diameter in the range of 500–800 nm and length of several tens of micrometers. From the EDX spectrum (inset in Fig. 2(a)), the atomic ratio of Cd:Te is estimated to be about 51:49, which is very close to the stoichiometric ratio of CdTe. Figure 2(c) displays the XRD pattern of the CdTe:Sb NWs. All the peaks could be properly assigned to CdTe with zinc blende structure (JCPDS 89-3053) and no obvious peak shift is observed, indicating the high phase purity of the product. XPS was used to further detect the compositions of the CdTe:Sb NWs, as shown in Figure 2(c). In addition to the peaks coming from Cd and Te, two Sb 3d peaks with binding energy of 530.5 eV and 540 eV, respectively, have appeared in the XPS spectrum. Considering that the CdTe:Sb NWs are uniform and clean with very few impurities and particles, the Sb peaks are most likely coming from the Sb element that incorporated into the NWs. From the typical HRTEM image and the corresponding fast Fourier transform (FFT) pattern of the CdTe:Sb NWs (Fig. 2(d)), it is found that the NWs have single crystal zinc blende structure with [211] growth orientation.

3.2. Electrical Transport Properties of the CdTe:Sb NWs

In order to determine the influence of Sb doping on the electrical transport properties of the CdTe:Sb NWs,

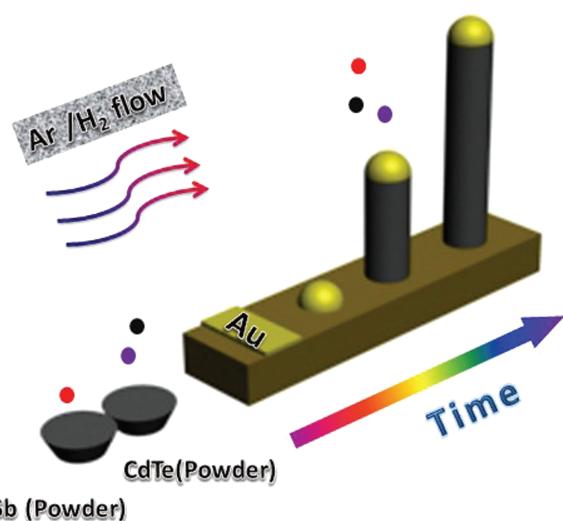


Fig. 1. Schematic illustration of the VLS growth process of the *p*-type CdTe:Sb NWs.

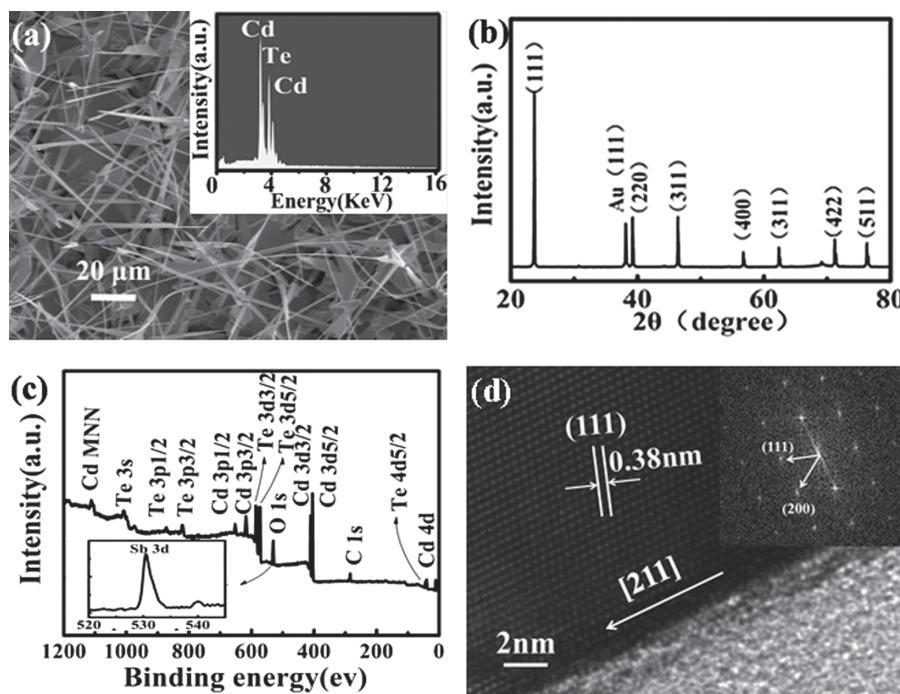


Fig. 2. (a) A typical FESEM image of the CdTe:Sb NWs. Inset shows the corresponding EDX spectrum. (b) XRD pattern of the CdTe:Sb NWs (sample 3). (c) XPS spectrum of the CdTe:Sb NWs (sample 3). Inset shows the enlarged Sb 3d_{5/2} and Sb 3d_{3/2} peaks. (d) HRTEM image of the CdTe:Sb NW. Inset shows the corresponding FFT pattern.

back-gate nanoFETs were constructed based on individual NWs (Figs. 3(a, b)). Figure 3(c) depicts the typical *I*–*V* curves of the CdTe NWs with different doping level. The ideal linearity of the *I*–*V* curves indicates the good ohmic contact between the CdTe NWs and the Cu/Au electrodes. It is noted that the intrinsic CdTe NW shows very low conduction current with a conductivity value as low as 1.5×10^{-5} S cm⁻¹. In contrast, the conduction current of the CdTe:Sb NWs has been significantly enhanced and the conductivities for sample 1, sample 2, and sample 3 are 2.4×10^{-3} , 1.3×10^{-2} and 0.33 S cm⁻¹, respectively. This result implies that the conductivity of the CdTe NWs could be tuned in a wide range of 4 orders of magnitude by adjusting the doping level. By applying the gate voltage (*V*_g) on the degenerately doped Si substrate beneath the SiO₂ dielectric layer in a bottom gate configuration, gate dependent source-drain current (*I*_{ds}) versus source-drain voltage (*V*_{ds}) curves of the CdTe NWs with different doping level were measured, as shown in Figures 3(d–f). For all the samples, the conductance of the NW monotonously increases (decreases) with the decreasing (increasing) of *V*_g, which is in good agreement with the typical behavior of a *p*-channel FET, revealing the *p*-type nature of the Sb-doped CdTe NWs. The *p*-type characteristic of the intrinsic CdTe NWs may originate from the native acceptor defects, such as Cd²⁺ vacancies and Te²⁻ at interstitial sites. However, the enhanced *p*-type conductivity for the CdTe:Sb NWs should be attributed to the substitutional doping of Sb³⁺ ions via replacing Te²⁻ ions. Our results unambiguously demonstrate that *p*-type doping has been

successfully achieved in the CdTe NWs and Sb could serve as an efficient dopant to tune the transport properties of the CdTe NWs.

The hole mobility (μ_h) of the CdTe NWs can be deduced from the transconductance (g_m) of the nanoFETs. Intercepting the linear part of the transfer characteristic curves, g_m can be calculated as follows:

$$g_m = \frac{dI_{ds}}{dV_g} \quad (1)$$

μ_h is thus given by:

$$\mu_h = \frac{dI_{ds}}{dV_g} \frac{\ln(4h/d)L}{2\pi\epsilon_0\epsilon_{SiO_2}V_{ds}} \quad (2)$$

where *L* is the channel length (15 μ m), *d* is NW diameter (800 nm), ϵ_{SiO_2} is the dielectric constant of the gate SiO₂ (~ 3.9), *h* is the thickness of SiO₂ (*h* = 300 nm). Based on the above equations, g_m for undoped NW, sample 1, sample 2 are calculated to be 0.01, 0.1, and 0.36 nS, respectively, at *V*_{ds} = -1 V. Correspondingly, μ_h are estimated to be 2.8×10^{-3} , 2.8×10^{-2} , and 0.1 cm² V⁻¹ s⁻¹, respectively. The enhanced hole mobility for NW with higher doping level is likely attributed to the improved electrode contact. On the other hand, we can obtain the hole carrier concentration (n_h) in the NWs to be 3.3×10^{16} , 5.3×10^{17} , and 8.1×10^{17} cm⁻³ for undoped NW, sample 1, and sample 2, respectively, according to the following relationship:

$$n = \frac{\sigma}{q\mu_h} \quad (3)$$

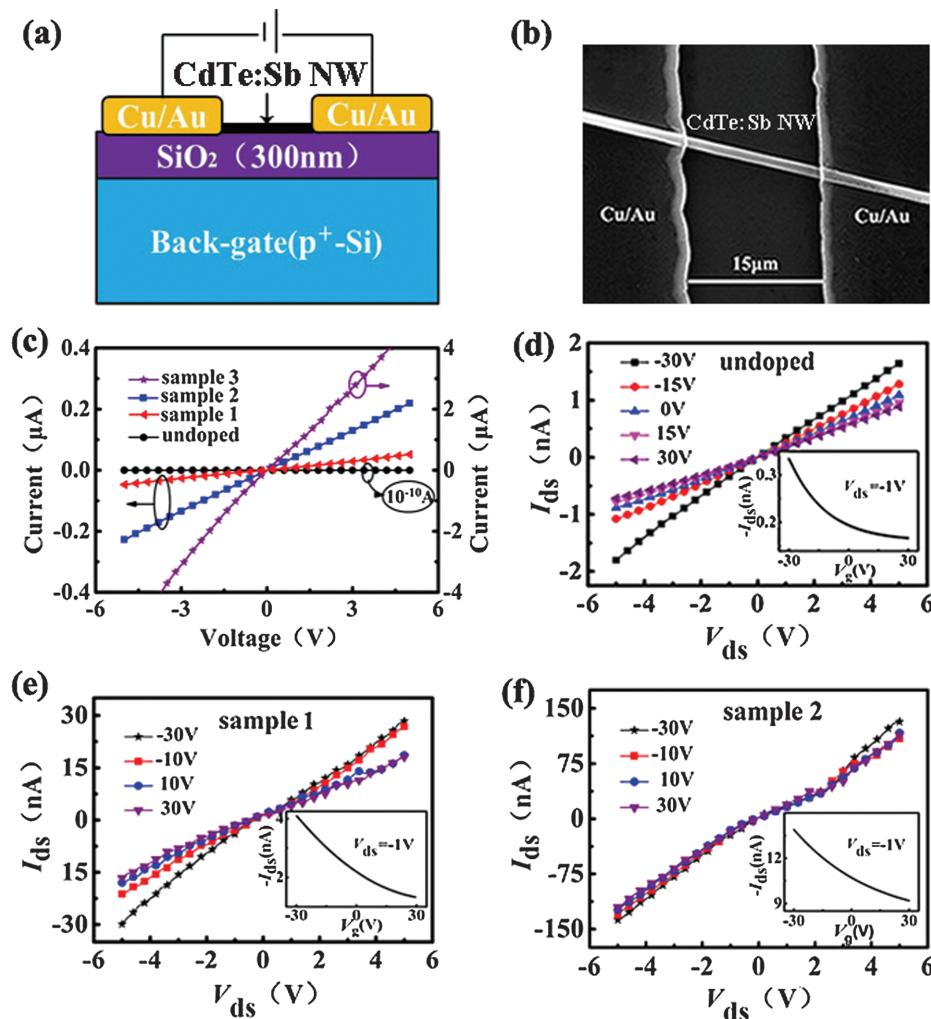


Fig. 3. (a) Schematic illustration of the back-gate nanoFET based on a single CdTe:Sb NW. (b) A representative FESEM image of the device. (c) Typical I - V curves of both the undoped and Sb-doped CdTe NWs. (d–f) are electrical transfer characteristics of undoped NW, sample 1, and sample 2, respectively. Insets show the I_{ds} - V_g curves measured at $V_{ds} = -1$ V.

where σ is the conductivity of the NW, and q is the elementary charge.

3.3. NanoSBDs Based on the CdTe:Sb NWs

In order to further exploit the potential applications of the CdTe:Sb NWs in the nanoelectronics, nanoSBDs based on individual NWs were constructed. Figure 4(a) shows the schematic illustration of the nanoSBDs, in which the Al electrode and Cu/Au electrode serve as the Schottky contact and the ohmic contact, respectively. Figure 4(b) displays the device characteristics of the nanoSBDs. Significantly, all the devices show a pronounced rectifying behavior. Further analysis indicates a low turn-on voltage of $\sim +1$ V and a high rectification ratio of $10^7\text{--}10^8$ for the devices. Measurements on three different nanoSBDs give the similar device characteristics (Fig. 4(b)), indicating the excellent reproducibility of the nanoSBDs. At room temperature, the thermionic emission will be the dominated

mechanism for the current transport in a Schottky diode. So, the I - V characteristic of the nanoSBD in the forward bias regime could be described by the following relationship:

$$I = I_0 \left[\exp\left(\frac{qV}{nkT}\right) - 1 \right] \approx I_0 \exp\left(\frac{qV}{nkT}\right) \quad (4)$$

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_b}{kT}\right) \quad (5)$$

where I_0 is the reverse saturation current, n the ideality factor, A the area of Schottky contact, A^* the effective Richardson constant, and Φ_b the Schottky barrier height. The ideality factor n can be obtained according to the formula $n = (q/kT)(dV/d\ln I)$ based on Eq. (4). From the semi-log I - V plots in the inset of Figure 4(b), n is estimated to be $1.60\text{--}1.67$ for the nanoSBDs. And $q\Phi_b$ is deduced to be ~ 0.82 eV from Eq. (5). This result is consistent with previous report, in which the contact barrier between Al and intrinsic CdTe was determined to be

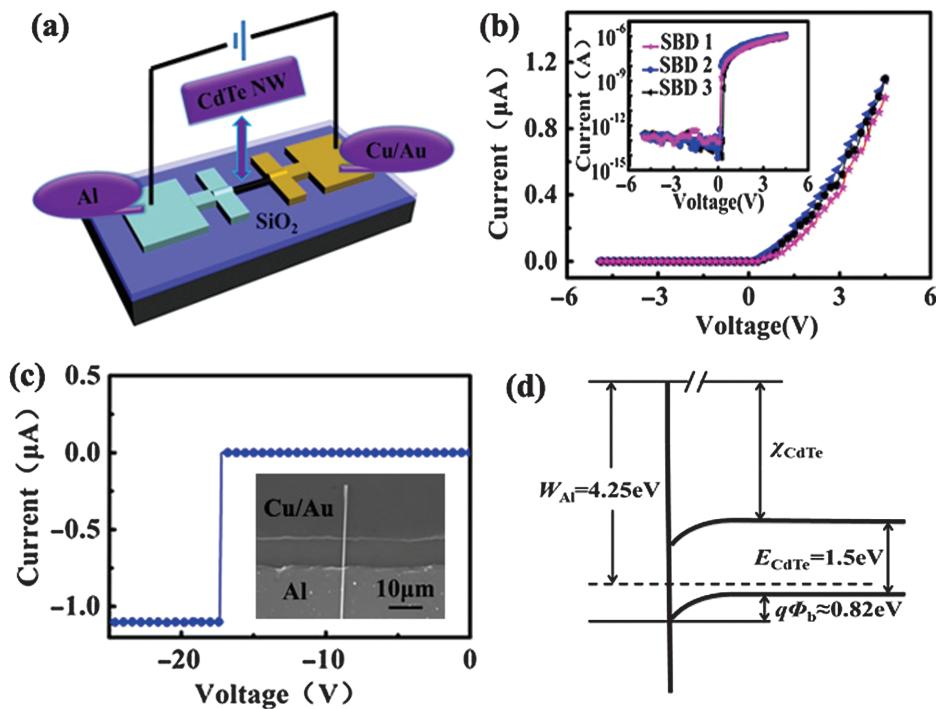


Fig. 4. (a) Schematic illustration of the Al/CdTe:Sb NW nanoSBD. (b) Rectifying characteristics of three different nanoSBDs, which are marked with SBD 1, SBD 2, and SBD 3. Inset shows the semi-log plots of the rectifying curves. (c) Avalanche breakdown curve of the nanoSBD at large reverse bias. Inset shows the typical SEM image of the nanoSBD based on an individual CdTe:Sb NW. (d) Energy band diagram of the Al/CdTe:Sb NW nanoSBD at zero bias, where W_{Al} represents the work function of Al films, χ_{CdTe} the electron affinity of CdTe, E_{CdTe} the band-gap of CdTe NW.

~0.76 eV.³⁰ On the other hand, at the reverse bias regime, the tunneling current is very low until a large reverse voltage (> -17.5 V) is applied, where a steep increase of the reverse current is observed. This phenomenon is associated with the avalanche breakdown mechanism at large reverse bias.³⁰ The large breakdown voltage for the device is a manifestation of the high performance of the devices. Figure 4(d) shows the energy band diagram of the Al/CdTe:Sb NW SBD. It is seen the energy bands of the *p*-type CdTe NW at the interface tend to bend upwards due to the difference in the work function with Al, thus leading to the formation of the contact barrier for holes transfer.

Besides the nanoSBDs on the SiO₂/Si substrates, flexible nanoSBDs were fabricated based on the CdTe:Sb NWs by adopting the PET flexible substrates. The device image is shown in Figure 5(a). It is seen that the device could be readily bent under the external force. Interestingly, the flexible nanoSBDs show similar device characteristics with the counterparts on the SiO₂/Si substrates and no evident degeneration in the device performance is observed. The turn-on voltage and switching ratio of the flexible nanoSBDs are deduced to be ~ +1 V and 10⁷, respectively. Moreover, the devices exhibit good resistance to the strains that were applied to the devices by bending the PET substrate with different curvatures. Measurements conducted under different strains of 0%, 0.1%, and 0.2% give the similar results (Fig. 5(b)), indicating that the

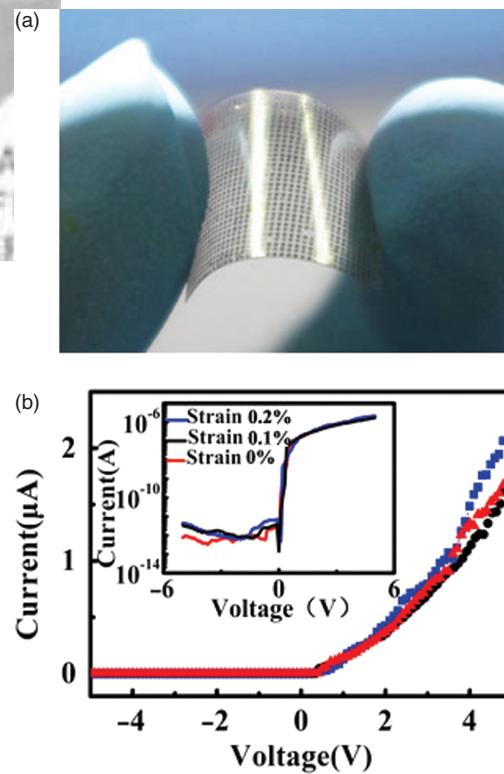


Fig. 5. (a) NanoSBDs fabricated on the flexible PET substrate. (b) Rectifying characteristics of the nanoSBDs on PET under different strains. Inset shows the semi-log plots of the rectifying curves.

CdTe:Sb NWs are promising candidate for the applications in flexible nanoelectronics.

4. CONCLUSIONS

In summary, single-crystal CdTe NWs with controlled *p*-type conductivity were synthesized by employing the Sb as the dopant. The efficient Sb doping in the CdTe NWs had led to a remarkable improvement on the NW's conductivity, which could be further tuned in a wide range of 4 orders of magnitude by adjusting the doping level. NanoSBDs based on single CdTe:Sb NW were constructed by using Al as the Schottky contact. The devices exhibit excellent diode characteristics with low turn on voltage of $\sim +1$ V, high rectification ratio of $>10^7$, and small ideality factor of ~ 1.67 . Moreover, flexible nanoSBDs fabricated by using PET as the substrates also showed the high device performance with good stability under strains. Our results demonstrated that the CdTe NWs with controlled Sb doping have promising applications in new-generation nanoelectronics.

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References and Notes

- Y. Jiang, W. J. Zhang, J. S. Jie, X. M. Meng, X. Fan, and S. T. Lee, *Adv. Funct. Mater.* 17, 1795 (2007).
- J. S. Jie, W. J. Zhang, Y. Jiang, X. M. Meng, Y. Q. Li, and S. T. Lee, *Nano Lett.* 6, 1887 (2006).
- Y. Jiang, X. M. Meng, J. Liu, Z. R. Hong, C. S. Lee, and S. T. Lee, *Adv. Mater.* 15, 1195 (2003).
- Z. W. Pan, Z. R. Dai, and Z. L. Wang, *Science* 291, 1947 (2001).
- Z. L. Wang and J. H. Song, *Science* 312, 242 (2006).
- E. Janik, P. Dluzewski, S. Kret, A. Presz, H. Kirmse, W. Neumann, W. Zaleszczyk, L. T. Baczevski, A. Petrouchik, E. Dynowska, J. Sadowski, W. Caliebe, G. Karczewski, and T. Wojtowicz, *Nanotechnology* 18, 475606 (2007).
- J. S. Jie, W. J. Zhang, Y. Jiang, X. M. Meng, J. A. Zapien, M. W. Shao, and S. T. Lee, *Nanotechnology* 17, 2913 (2006).
- X. W. Zhang, J. S. Jie, Z. Wang, C. Y. Wu, L. Wang, Q. Peng, Y. Q. Yu, P. Jiang, and C. Xie, *J. Mater. Chem.* 18, 6736 (2011).
- D. Wu, Y. Jiang, S. Y. Li, F. Z. Li, J. W. Li, X. Z. Lan, Y. G. Zhang, C. Y. Wu, L. B. Luo, and J. S. Jie, *Nanotechnology* 22, 405201 (2011).
- H. Z. Zhong, Y. Zhou, Y. Yang, C. H. Yang, and Y. F. Li, *J. Phys. Chem.* 17, 6538 (2007).
- X. N. Wang, H. J. Zhu, Y. M. Xu, H. Wang, Y. Tao, S. K. Hark, X. Xiao, and Q. Li, *ACS Nano* 5, 3302 (2010).
- T. L. Zhang, X. Y. Sun, and B. Liu, *Spectrochimica Acta Part A* 79, 1566 (2011).
- S. M. Zhou, X. H. Zhang, X. M. Meng, S. K. Wu, and S. T. Lee, *Appl. Phys. A* 81, 1647 (2005).
- M. Kuno, O. Ahmad, V. Protasenko, D. Bacinello, and T. H. Kosel, *Chem. Mater.* 18, 5722 (2006).
- Q. Yang, K. Tang, C. Wang, Y. Qian, and S. Zhang, *J. Phys. Chem. B* 106, 9227 (2002).
- Z. Tang, N. A. Kotov, and M. Giersig, *Science* 297, 237 (2002).
- D. Xu, D. Chen, Y. Xu, X. Shi, G. Guo, L. Gui, and Y. Tang, *Pure Appl. Chem.* 72, 127 (2000).
- A. W. Zhao, G. W. Meng, L. D. Zhang, T. Gao, S. H. Sun, and Y. T. Pang, *Appl. Phys. A* 76, 537 (2003).
- T. Ohgai, L. Gravier, X. Hoffer, and J. P. Ansermet, *J. Appl. Electrochem.* 35, 479 (2005).
- M. Sima, I. Enculescu, C. Trautmann, and R. Neumann, *J. Optoelectron. Adv. Mater.* 6, 121 (2004).
- S. H. Hur, O. O. Park, and J. A. Rogers, *Appl. Phys. Lett.* 86, 243502 (2005).
- Q. Cao, S. H. Hur, Z. T. Zhu, Y. Sun, C. Wang, M. A. Meitl, M. Shim, and J. A. Rogers, *Adv. Mater.* 18, 304 (2007).
- S. J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M. A. Alam, S. V. Rotkin, and J. A. Rogers, *Nat. Nanotechnol.* 2, 230 (2007).
- Q. Cao, H. Kim, N. Pimparkar, J. P. Kulkarni, C. Wang, M. Shim, K. Roy, M. A. Alam, and J. A. Rogers, *Nature* 454, 495 (2008).
- F. N. Ishikawa, H. Chang, K. Ryu, P. Chen, A. Badmaev, L. G. D. Arco, G. Shen, and C. Zhou, *ACS Nano* 3, 73 (2009).
- S. Kim, J. Park, S. Ju, and S. Mohammadi, *ACS Nano* 4, 2994 (2010).
- L. Jiao, X. Xian, Z. Wu, J. Zhang, and Z. Liu, *Nano Lett.* 9, 205 (2009).
- J. O. Hwang, D. H. Lee, J. Y. Kim, T. H. Han, B. H. Kim, M. Park, K. No, and S. O. Kim, *J. Mater. Chem.* 21, 3432 (2011).
- W. F. Zhang, Z. B. He, G. D. Yuan, J. S. Jie, L. B. Luo, X. J. Zhang, Z. H. Chen, C. S. Lee, W. J. Zhang, and S. T. Lee, *Appl. Phys. Lett.* 94, 123103 (2009).
- S. M. Sze and K. K. Ng, *Physics of Semiconductor Devices*, Wiley-Interscience (2006).