High-performance nonvolatile Al/AlO_x/CdTe:Sb nanowire memory device

2013 Nanotechnology 24 355203

(http://iopscience.iop.org/0957-4484/24/35/355203)

Nanotechnology **24** (2013) 355203 (7pp) doi:10.1088/0957-4484/24/35/355203

High-performance nonvolatile Al/AlO$_x$/CdTe:Sb nanowire memory device

Chao Xie[1,2], Biao Nie[2], Long Zhu[2], Long-Hui Zeng[2], Yong-Qiang Yu[2], Xian-He Wang[2], Qun-Ling Fang[3], Lin-Bao Luo[2] and Yu-Cheng Wu[1]

[1] School of Materials Science and Engineering, Hefei University of Technology, Hefei, Anhui 230009, People's Republic of China
[2] School of Electronic Science and Applied Physics and Anhui Provincial Key Laboratory of Advanced Functional Materials and Devices, Hefei University of Technology, Hefei, Anhui 230009, People's Republic of China
[3] School of Medical Engineering, Hefei University of Technology, Hefei, Anhui 230009, People's Republic of China

E-mail: luolb@hfut.edu.cn and ycwu@hfut.edu.cn

Received 14 May 2013, in final form 27 June 2013
Published 7 August 2013
Online at stacks.iop.org/Nano/24/355203

Abstract
Here we demonstrate a room temperature processed nonvolatile memory device based on an Al/AlO$_x$/CdTe:Sb nanowire (NW) heterojunction. Electrical analysis shows an echelon hysteresis composed of a high-resistance state (HRS) and a low-resistance state (LRS), which can allow it to write and erase data from the device. The conductance ratio is as high as 10^6, with a retention time of 3×10^4 s. Moreover, the SET voltages ranged from +6 to +8 V, whilst the RESET voltage ~0 V. In addition, flexible memory nano-devices on PET substrate with comparable switching performance at bending condition were fabricated. XPS analysis of the Al/AlO$_x$/CdTe:Sb NW heterojunction after controlled Ar^+ bombardment reveals that this memory behavior is associated with the presence of ultra-thin AlO$_x$ film. This Al/AlO$_x$/CdTe:Sb NW heterojunction will open up opportunities for new memory devices with different configurations.

(Some figures may appear in colour only in the online journal)

1. Introduction

Cadmium telluride (CdTe), as a typical semiconductor material of the II–VI group, has received intensive research interest over recent decades due to its unique electrical and optical properties [1, 2]. For example, CdTe has a direct bandgap of 1.5 eV which is the optimum bandgap for photovoltaic device applications. Furthermore, it is an excellent light harvester with a high absorption coefficient in the whole solar energy spectrum. For this reason, CdTe has become one of the most important photovoltaic materials, with a theoretical efficiency as high as 30%. Although its market share accounts for about 6% of the global photovoltaic market, second only to silicon [3, 4], CdTe is the most popular photovoltaic material for aerospace purposes, especially in space shuttles, spacecraft, and man-made satellites, where efficient generation of electricity is vitally important for various complicated instruments [5]. In addition, due to its high atomic number, as well as high electron mobility, CdTe is the primary semiconductor material for room-temperature x-ray and gamma-detectors [6].

Compared with their thin film and bulk counterparts, CdTe nanostructures in one-dimensional (1D) form (e.g., nanowires [7], nanotubes [8, 9], nanoribbons [10], etc) have exhibited improved electrical and optical properties. To date, considerable efforts have been made with respect to the fabrication of 1D nanostructures with desired shapes and sizes via the hydrothermal method [11], solvothermal route [12], chemical vapor deposition (CVD) [13], porous anodized aluminum oxide (AAO) template [14], and pulsed

laser deposition (PLD) [15]. Based on these nanostructures, light-emitting devices (LEDs) [16], photonic crystals [17], nonlinear optical devices [18], and biological labels with high performance have been reported [19]. In spite of the enormous progress in synthesis and device application, there is a sparsity of research activity dealing with memory devices, which are normally used to retain stored information, as has been successfully achieved on other II–VI semiconductor nanostructures, such as ZnO nanorods [20, 21], ZnS nanoribbons [22], CdS nanoribbon [23], CdSe nanowires [24, 25], and so on.

In this contribution, we present the fabrication of a nonvolatile memory device based on a sandwich-like Al/AlO_x/CdTe:Sb nanowire (NW) junction. Electrical analysis reveals that the as-fabricated nano-device exhibits excellent memory characteristics, with a conductance ratio of up to 10^6. What is more, it has a retention time of over 3×10^4 s. A memory device assembled on a flexible polyethylene terephthalate (PET) substrate shows similar device performance with excellent reproducibility. X-ray photoemission spectroscopy (XPS) study after thinning down indicates that the memory behavior can be ascribed to the formation of an ultra-thin layer of AlO_x during Al deposition at a low deposition rate. It is expected that such a nonvolatile memory device based on Al/AlO_x/CdTe:Sb NW would open up new opportunities in future electronics devices.

2. Experimental section

2.1. Synthesis and characterization of CdTe:Sb NWs

The Sb doped CdTe NWs were synthesized in a horizontal quartz tube furnace using a thermal co-evaporation method. Detailed description of the synthesis was reported in our previous work [26]. After growth, the Si substrates containing a layer of black wool-like product were taken out of the furnace. The microstructures of the as-synthesized CdTe:Sb NWs were studied by field emission scanning electron microscope (FESEM, Philips XL 30 GEG), transmission electron microscope (TEM, Philips CM20, operating at 200 kV) and high-resolution transmission electron microscopy (HRTEM, JEOL JEM-2010, operating at 200 kV). The chemical composition of the sample was analyzed by XPS which was carried out on a VG ESCALAB 220i-XL surface analysis system equipped with a monochromatic Al x-ray (1486.6 eV) source. To study the valence state of Al at the Al/CdTe:Sb NW contact, the 40 nm thick Al film on NWs was successively thinned down by 5 and 30 nm via Ar^+ bombardment.

2.2. Fabrication and analysis of Al/AlO_x/CdTe:Sb NW junction memory device

To fabricate nonvolatile memory devices, the above CdTe:Sb NWs were firstly dispersed uniformly onto SiO_2 (300 nm)/p^+-Si substrates at a desired density. Then an electron-beam evaporator was employed to deposit Cu (4 nm)/Au (50 nm) metal electrodes on one end of the NW, and AlO_x/Al (40 nm)

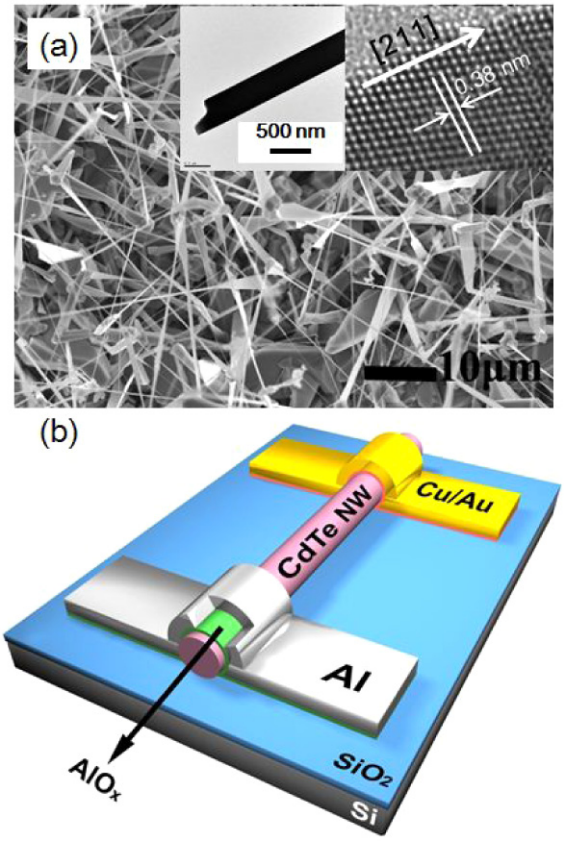

Figure 1. (a) SEM image of the as-synthesized CdTe:Sb NW, the left inset is a TEM image of an individual Sb doped CdTe NW, the right inset shows the corresponding HRTEM image. (b) Schematic illustration of a nonvolatile memory device based on Al/AlO_x/CdTe:Sb NW.

electrodes on the other end (the deposition rate and pressure were set to be 0.5 Å s^{-1} and 2×10^{-4} Pa, respectively). Please note that at the initial deposition stage (∼0–5 nm), both deposition rate and pressure were intentionally adjusted to 0.1 Å s^{-1} and 5×10^{-3} Pa, respectively, in favor of the formation of Al oxide. In this study, flexible memory devices on flexible PET substrates were also constructed by a similar process. The electrical measurement of the device was performed on a semiconductor characterization system (Keithley 4200-SCS).

3. Results and discussion

The as-grown NW was then directly transferred into the FESEM chamber for morphology characterization. As exhibited in figure 1(a), the Si wafer is fully covered by wire-like nanostructures with lengths of tens of micrometers. Figure 1(b) shows a representative dark-field TEM image, in which a 500 nm thick NW with a smooth surface can be easily visualized. The lattice fringes in the inset HRTEM image reveal the zinc blende single-crystal characteristics of the NWs. In addition, the *d*-spacing between the adjacent lattice planes is determined to be 0.38 nm, indicative of the [211] growth direction of the NW. To explore the capability of the as-prepared CdTe:Sb NWs for nonvolatile memory application, asymmetric Al/CdTe:Sb NW/Cu/Au junction, as

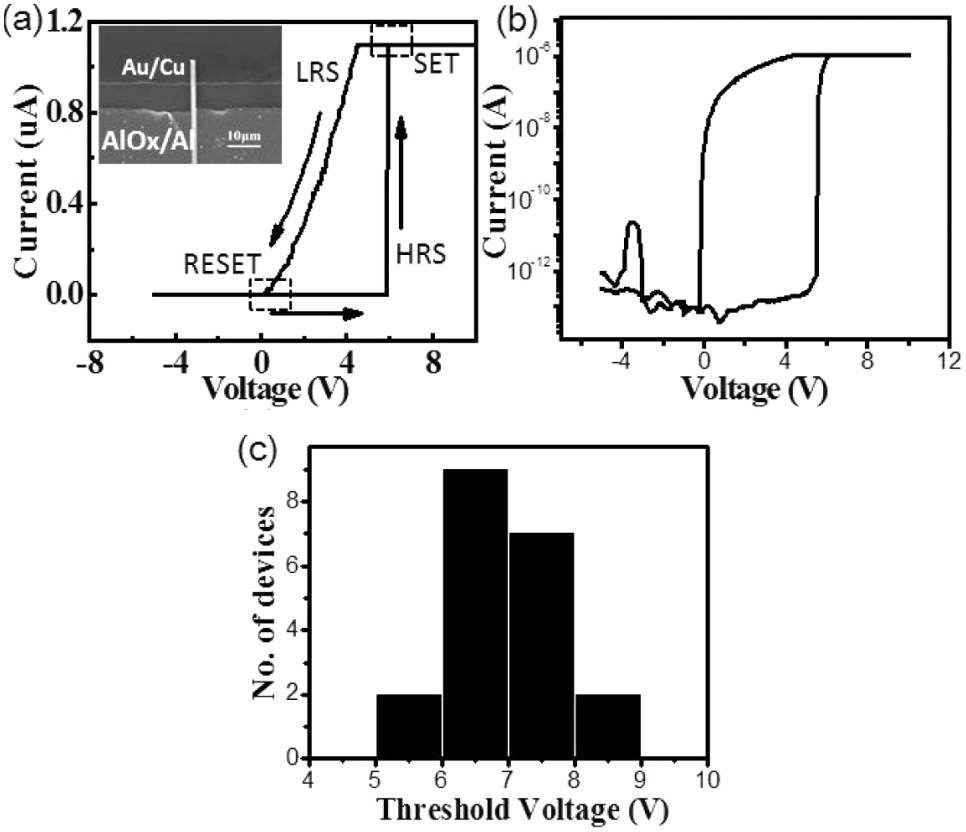

Figure 2. (a) Switching characteristics of the Al/AlO_x/CdTe:Sb NW junction, where the LRS and HRS indicate the low and high conduction states as the ON and OFF states, respectively. The inset is a typical FESEM image of the memory device. Note that the Au/Cu electrode was grounded during analysis. (b) The semi-log plot of the hysteresis behavior. (c) Statistical distribution of the threshold voltage of 20 devices.

schematically illustrated in figure 1(b), was fabricated. Note that during device fabrication, the 40 nm thick Al film was intentionally deposited slowly at the initial stage (0–5 nm), which is highly favorable for the oxidation of Al.

To examine the electrical properties of the Al/AlO_x/CdTe:Sb NW/Cu/Au junction, we firstly studied the current evolution on both linear and semi-logarithmic scales (figures 2(a) and (b)). It is interesting to find that when the bias voltage was scanned from -5 to 10 V and back to -5 V, an echelon hysteresis composed of a high-resistance state (HRS or OFF) and a low-resistance state (LRS or ON) appears. This phenomenon is completely different from the Al/CdTe:Sb NW/Cu/Au junction, in which excellent rectifying behavior with low turn-on voltage of $\sim+1$ V and a high rectification ratio of 10^7–10^8 was observed [27]. Significantly, this switching process can enable the Al/AlO_x/CdTe:Sb NW junction to function as an efficient memory device, which is characterized by writing and erasing information from the device. For a typical device operation process, this device can serve to write information into the device as a nonvolatile ON state is achieved. Conversely, when the nonvolatile OFF state is achieved, it can serve to erase data from the device (for the sake of clarification, we here define the SET process from HRS to LRS, while the RESET process from LRS to HRS). This observation is interesting as it is the first nano memory device composed of p-type semiconductor nanostructures ever reported [28, 29]. The memory device shows excellent scalability and reproducibility that makes it suitable for future device applications. Figure 2(c) shows the statistical distribution of the threshold voltage of 20 devices by a similar process, according to which the majority of the threshold voltages lie in the range from $\sim$6 to 8 V.

Next, we examined the retention performance by applying pulses of $\pm$10 V to switch the conduction state between HRS and LRS. Figure 3(a) shows the retention characteristics of the ON and OFF states of the memory device measured at $V = 3$ V. It can be seen that a high conductance ratio of 10^6 can be stably retained for 3×10^4 s. This conductance ratio is the highest ever reported. What is more, the retention time is shorter than the device composed of carbon nanotube [25], but much longer than other devices composed of CdSe:Ga NW [26], Si NW [27], ZnO NW [28], and In_2O_3 NW [29]. The detailed comparison of device performance is summarized in table 1. To further reveal the capability for memory application, a pulsed voltage was applied for the SET and RESET process. Figure 3(b) shows the switching endurance under a read voltage of 3 V. Apparently, one can see that the memory device can be reversibly switched between the ON and OFF states. Even after 30 cycles, both R_{on} and R_{off} keep almost unchanged, indicative of great potential for future programmable logic element applications.

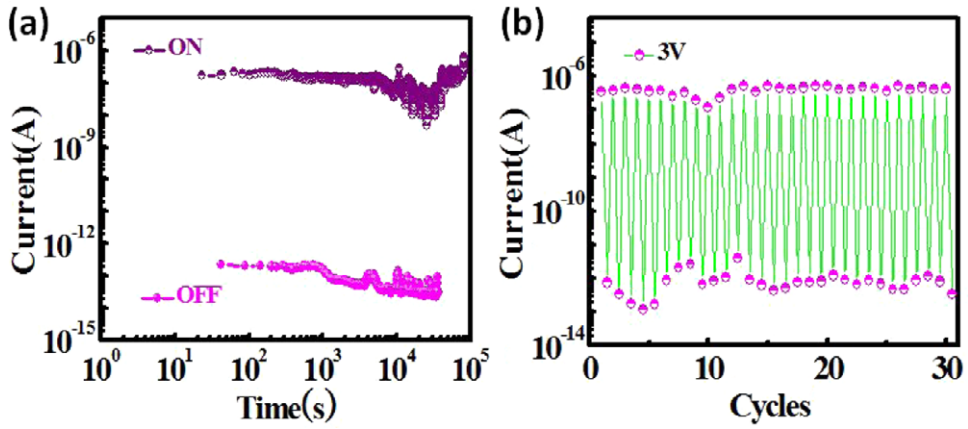

Figure 3. (a) Retention characteristics of memory device measured at $V = 3$ V; the device was switched ON using $+10$ V, and was switched OFF using -10 V. (b) Bistable resistance for the HRS and LRS as a function of switching cycles.

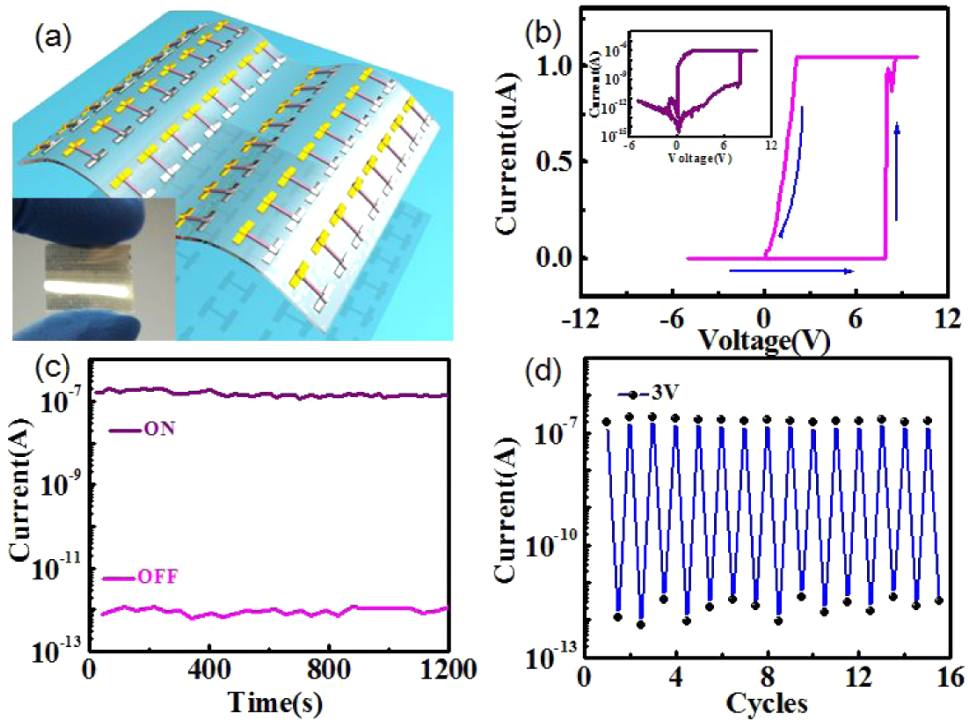

Figure 4. (a) Schematic illustration of the Al/AlO$_x$/CdTe:Sb NW memory device fabricated on the flexible PET substrate. Inset shows the digital camera picture of the as-fabricated flexible nano-devices. (b) Resistive switch characteristics of the memory device on a PET substrate. (c) Retention times for the Al/AlO$_x$/CdTe:Sb NW device measured at $V = 3$ V; the device was switched ON using $+10$ V, and was switched OFF using -10 V. (d) Bistable resistance for the HRS and LRS as a function of switching cycles.

Table 1. Summary of device performance of similar semiconductor nanostructure based memory devices.

	Resistance ON/OFF ratio	Retention time (s)
Our work	~6 order	3×10^4
Carbon nanotube [30]	~4 order	10^5
CdSe:Ga nanowire [24]	~4 order	10^4
ZnO nanowire [31]	~5 order	10^4
Silicon nanowire [32]	~4 order	1.2×10^3
In_2O_3 nanowire [33]	~4 order	1.2×10^4

It is noted that similar memory characteristics can be observed on flexible Al/AlO$_x$/CdTe:Sb NW heterojunctions as well. Figure 4(a) shows a typical schematic illustration of the memory device on a flexible PET film, which could be readily bent under external force (inset of figure 4(a)). Interestingly, the flexible memory devices show similar device characteristics. The 'SET' and 'RESET' voltages are determined to be ~8 and 0 V, respectively, comparable to that without bending. Additionally, the 'ON' and 'OFF' currents are about 10^{-7} and 10^{-12} A, respectively, yielding a current R_{on}/R_{off} of about 10^5. Notably, the HRS/LRS resistance ratio

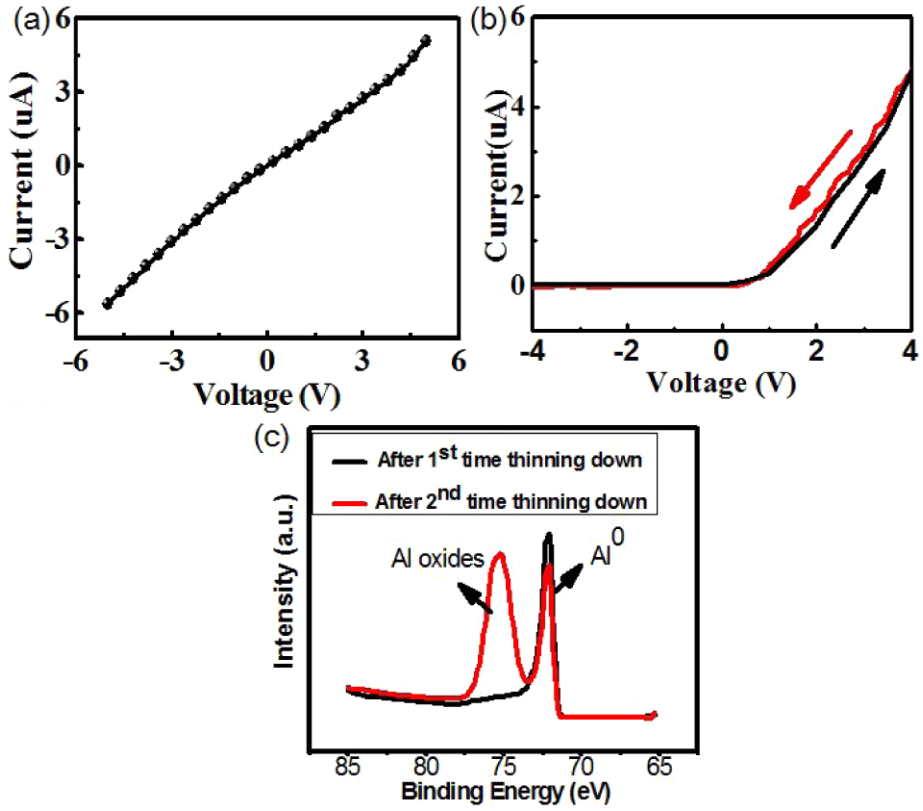

Figure 5. (a) *I–V* curve of an Sb doped CdTe NW with two Cu/Au electrodes on both ends. (b) The typical *I–V* curve of the Al/CdTe:Sb NW Schottky junction with a dual sweep. (c) XPS spectra for Al peaks at high resolution.

remains constant even after a long retention time of 1.2×10^3 s. Moreover, the R_{on} and R_{off} shown in figure 4(d) for the first 15 cycles are very stable, suggesting good potential for applications in future flexible electronics.

Although it is difficult to ascertain the cause of this phenomenon at this stage, it is certain that this observed memory characteristic should not be ascribed to the CdTe:Sb NW/Cu/Au, as good contact (Ohmic contact) was formed between the Au/Cu and CdTe:Sb NW (figure 5(a)). On the other hand, Al/CdTe:Sb NW Schottky junction cannot give rise to this memory behavior either. Figure 5(b) displays a typical *I–V* curve of the Al/CdTe Schottky junction, whose Al electrode was deposited at a constant rate of 0.5 Å s^{-1}. It is seen that the current versus voltage virtually overlaps when the voltage is swept from −4 to 4 V then back to −4 V, suggesting no hysteresis for such structure. This finding is interesting in that a slight change in deposition rate of Al can considerably affect the electrical properties of the Schottky junction. To further unveil the underlying reasons for this hysteresis, we studied the interfacial composition of the Al/CdTe:Sb NW using the XPS technique. Figure 5(c) compares the Al 2p spectra coated with a layer of 40 nm Al metal after Ar^+ bombardment for different durations. It can be found that there is only one single peak at 72 eV, ascribable to Al^0 when the sample was pared down by ∼5 nm. However, after further thinning down the Al film by 30 nm, one more peak at 72 eV due to Al oxide can be easily observed. This result confirms the formation of AlO_x film between the NW and Al at low deposition rate. In fact, as we will discuss later, it is this interfacial AlO_x thin film that is responsible for writing and erasing data when applied bias voltage.

Previously, Panda *et al* have successfully fabricated oxide-based nonvolatile memory devices with excellent memory characteristics in terms of high-resistance ratio, long retention time and good stability [34, 35]. They found that the memory behavior can be explained well by switchable formation and dissolution of conducting filament resultant from movement of oxygen vacancies [36, 37]. Unfortunately, this model is not applicable to our Al/AlO_x/CdTe NW memory device in that oxygen vacancies in the AlO_x thin layer can hardly move to form conducting filaments. In light of this, we propose a new model shown in figure 6 to interpret the nonvolatile memory characteristics. The device functions like a floating gate memory due to the existence of the oxide layer at the junction interface. The oxygen vacancies in the oxide layer can serve as trapping centers for electrons. When a forward voltage is applied across the junction, electrons drift from the Al to the interfacial oxide layer and are then trapped by oxygen vacancies, leading to reduced Schottky barrier height and thus turning the memory device to the 'ON' state (LRS) (figure 6(a)), which corresponds to the writing of data into the device. In contrast, when a reverse voltage is applied, electrons trapped by oxygen vacancies will be injected into the Al, giving rise to an increased barrier height. This increase in barrier height will lead to an 'OFF' state

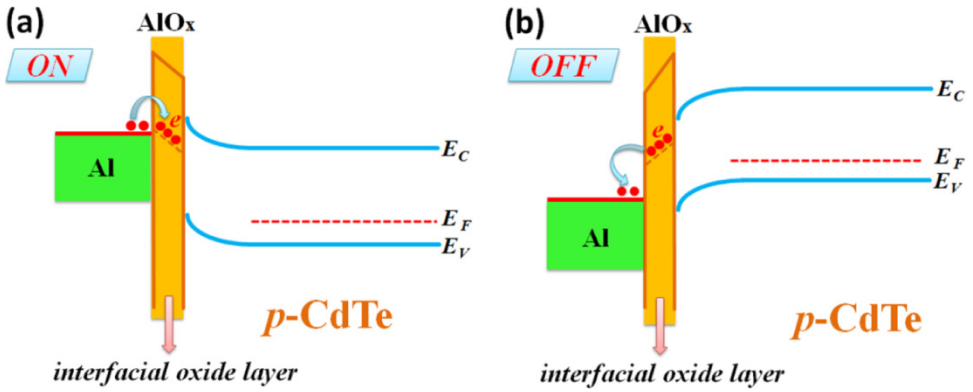

Figure 6. (a) Schematic energy band diagram for the Al/CdTe:Sb Schottky junction in the ON state when a forward bias is applied to the Cu/Au electrode. The electrons are trapped in the interface states. (b) Schematic energy band diagram for the device in the OFF state when a reverse bias is applied to the Cu/Au electrode. The trapped electrons are released to the Al.

(HRS) for the memory, corresponding to erasing data from the device (figure 6(b)).

Conclusion

In summary, we report on the fabrication of a nonvolatile memory device based on an Al/AlO_x/CdTe:Sb NW heterojunction. Device analysis shows that the as-fabricated nano-device exhibits excellent memory characteristics, with a conductance ratio of up to 10^6. Moreover, it has a retention time of over 3×10^4 s. Remarkably, flexible memory devices on PET film at bending condition exhibited similar memory characteristics as well. Further XPS study and controlled experiment reveals that this memory behavior can be ascribed to the presence of the ultra-thin AlO_x film that is formed at low deposition rate. The observed oxide layer induced memory behavior will not only help provide a new insight into the working mechanism but also facilitate the development of new types of memory device with high performance.

Acknowledgments

This work was supported by the National Natural Science Foundation of China (NSFC, Nos 51172151, 21101051, 21205026, 91023030, 51072044), and the Fundamental Research Funds for the Central Universities (2012HGCX0003).

References

[1] Jie J S, Zhang W J, Bello I, Lee C S and Lee S T 2010 *Nano Today* **5** 313
[2] Neretina S, Hughes R A, Britten J F, Sochinskii N V, Preston J S and Mascher P 2007 *Nanotechnology* **18** 275301
[3] Boettcher S W, Spurgeon J M, Putnam M C, Warren E L, Turner-Evans D B, Kelzenberg M D, Maiolo J R, Atwater H A and Lewis N S 2010 *Science* **327** 185
[4] Xie C *et al* 2011 *Appl. Phys. Lett.* **99** 133113
[5] Miles R W, Hynes K M and Forbes I 2005 *Prog. Cryst. Growth Charact. Mater.* **51** 1
[6] Zhou S M, Zhang X H, Meng X M, Wu S K and Lee S T 2005 *Appl. Phys.* A **81** 1647
[7] Tang Z Y, Kotov N S and Giersig M 2002 *Science* **297** 237
[8] Ding J, Wang X, Zhuo L H and Tang B 2009 *J. Mater. Chem.* **19** 3027
[9] Niu H J and Gao M Y 2006 *Angew. Chem. Int. Edn* **45** 6462
[10] Xie X *et al* 2012 *Nanoscale* **4** 2914
[11] Cao X B, Lan X M, Guo Y and Zhao C 2008 *Cryst. Growth Des.* **8** 575
[12] Yu W W, Wang Y A and Peng X G 2003 *Chem. Mater.* **15** 4300
[13] Wang X N, Wang J, Zhou M J, Zhu H J, Wang H, Cui X D, Xiao X D and Li Q 2009 *J. Phys. Chem.* C **113** 16951
[14] Kum M C, Yoo Y B, Rheem Y W, Bozhilov K N, Chen W, Mulchandani A and Myung N M 2008 *Nanotechnology* **19** 325711
[15] Neretina S, Hughes R A, Sochinskii N V, Weber M, Lynn K G, Wojcik J, Pearson G N, Preston J S and Mascher P 2006 *J. Vac. Sci. Technol.* A **24** 606
[16] Chen W, Grouquist D and Roark J 2002 *J. Nanosci. Nanotechnol.* **2** 47
[17] Mak J S W, Farah A A, Chen F F and Helmy A S 2011 *ACS Nano* **5** 3823
[18] Pan L Y, Tamai N, Kamada K and Deki S 2007 *Appl. Phys. Lett.* **91** 051902
[19] Maestro L M, Jacinto C, Silva U R, Cetrone F, Capobianco J A, Jaque D and Sole J G 2011 *Small* **7** 1774
[20] Yoon J *et al* 2011 *ACS Nano* **5** 558
[21] Yeom D, Kang J, Lee M, Jang J, Yun J, Jeong D Y, Yoon C, Koo J and Kim S 2008 *Nanotechnology* **19** 395204
[22] Yu Y Q, Jiang Y, Jiang P, Zhang Y G, Wu D, Zhu Z F, Liang Q, Chen S R, Zhang Y and Jie J S 2013 *J. Mater. Chem.* A **1** 1238
[23] Wu P C, Dai Y, Ye Y, Fang X L, Sun T, Liu C and Dai L 2010 *J. Mater. Chem.* **20** 4404
[24] Wu D, Jiang Y, Yu Y Q, Zhang Y G, Li G H, Zhu Z F, Wu C Y, Wang L, Luo L B and Jie J S 2012 *Nanotechnology* **23** 485203
[25] He Z B *et al* 2010 *J. Phys. Chem.* C **114** 4663
[26] Xie C, Luo L B, Zeng L H, Chen J J, Nie B, Hu J G, Wu C Y, Wang L and Jie J S 2012 *Cryst. Eng. Commun.* **14** 7222
[27] Zhu L, Jie J S, Wu D, Luo L B, Wu C Y, Zhu Z F, Yu Y Q and Wang L 2012 *J. Nanoeng. Nanomanuf.* **2** 191
[28] Lee J J and Kwong D L 2005 *IEEE Trans. Electron Devices* **52** 507
[29] Wang Q, Song Z T, Liu W L, Lin C L and Wang T H 2004 *Appl. Surf. Sci.* **230** 8
[30] Manohara H M, Wong E W, Schlecht E, Hunt B D and Siegel P H 2005 *Nano Lett.* **5** 1469

[31] Sohn J I, Choi S S, Morris S M, Bendall J S, Coles H J, Hong W K, Jo G H, Lee T H and Welland M E 2010 *Nano Lett.* **10** 4316
[32] Duan X F, Huang Y and Lieber C M 2002 *Nano Lett.* **2** 487
[33] Zhang W F, Jie J S, Luo L B, Yuan G D, He Z B, Yao Z Q, Chen Z H, Lee C S, Zhang W J and Lee S T 2008 *Appl. Phys. Lett.* **93** 183111
[34] Panda D, Huang C Y and Tseng T Y 2010 *Appl. Phys. Lett.* **100** 112901
[35] Panda D, Dhar A and Ray S K 2010 *J. Appl. Phys.* **108** 104513
[36] Panda D, Dhar A and Ray S K 2012 *IEEE Trans. Nanotechnol.* **11** 51
[37] Panda D and Tseng T Y 2013 *Thin Solid Films* **531** 1