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Ultrahigh Mobility of p-Type CdS Nanowires: Surface Charge Transfer Doping and Photovoltaic Devices

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Low-dimensional single-crystalline semiconductor nanostructures have emerged as ideal building blocks in various powerful nano-devices due to their superior optical, physical and electrical properties over traditional thin film and bulk materials.[1,2] Cadmium sulfide (CdS), as an important II–VI semiconductor with a wide direct band-gap of 2.42 eV at room temperature,[3] is of particular interest as it can function as important building blocks for wide-ranging nano-electronic and nano-optoelectronic devices. Thus far, low-dimensional CdS nanostructures, such as quantum dots (QDs), nanowires (NWs), nanoribbons (NRs), and nanotubes (NTs), have been successfully prepared using thermal evaporation,[4] solvothermal process,[5] polymer-assisted chemical method and so on.[6] Based on these CdS nanostructures, a wide range of nano-devices and nano-systems, including metal semiconductor field-effect transistors (MESFETs),[7] logic circuits,[8] Schottky junction diode,[9] hydrogen generator,[10] and solar cell[11,12] have been explored.

Undoubtedly, the operation of the CdS based nano-devices mentioned above relies on the density of free charge carriers available in the semiconductor nanostructures. In general, the modulation of the electrical properties is achieved by traditional doping method, namely, intentionally introducing impurity atoms into the host lattice of semiconductor. For example, Ma et al. initiated the n-type doping of CdS nanobelts by using an in-situ indium (In) doping method in chemical vapor deposition, the as-doped CdS nanostructure revealed an electron concentration and mobility as high as 2.4×10^{16} cm^{-3} and 146 cm^2/Vs, respectively.[13] Besides In, other elements such as P,[14,15] N,[16] Cl,[17] and Ga[18,19] have also proved to be effective dopants for achieving high-concentration n-type CdS doping. In contrast to the facile n-type doping, p-type doping of CdS nanostructures has been extraordinarily difficult and thus have never been achieved, except for some works on theoretical prediction.[20,21] This difficulty mainly arises from the strong self-compensation effect, that is, doping of the acceptors will inevitably introduce one or more donor defects in the lattice, such as the sulfur vacancies, thus counteracting the effect of p-type doping. The low solubility of dopants and the deep acceptor level also impede the realization of effective p-type doping in CdS.[22,23] In addition to CdS, similar unipolar characteristic is commonly observed on the II–VI semiconductors such as ZnO, CdSe and ZnTe (**Table 1**). Without question, the failure in producing both n- and p-type semiconductors with good stability and reproducibility has constituted the main obstacle to development of II–VI semiconductors based optoelectronic devices (e.g., light-emitting diodes, laser).

Herein, we report the first experimental realization of p-type CdSNWs *via* a simple surface charge transfer doping technique, which is characterized by spontaneous electron exchange as a result of the remarkable differences in Fermi levels.[30] The undoped CdSNW (u-CdSNW) after surface decoration with a thin MoO_3 layer exhibited pronounced p-type conduction behavior, with a record hole mobility of 2035 cm^2/Vs. Detailed mechanism on the surface charge transfer process and electrical transport characteristics at low temperature was elucidated. Furthermore, selective deposition on the half part of a n-type CdSNW led to the realization of CdSNW p-n homojunction, which exhibited pronounced photovoltaic behavior with energy conversion efficiency as high as 1.65% under light illumination. Our results indicate that such a surface charge

Table 1. Summary of the doping of several unipolar II–VI 1-D nanostructured semiconductors.

	p-type doping	n-type doping
CdS	/	In,[13] P,[14,15] N,[16] Cl,[17] Ga,[18,19] etc.
CdSe	/	In,[24] Ga,[25] Cd,[26] etc.
ZnTe	Sb,[27] Cu,[28] N,[29] etc.	/

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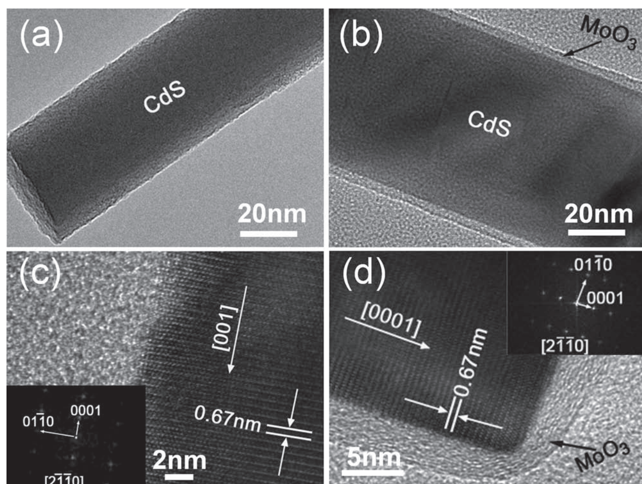

Figure 1. (a) TEM image of a u-CdSNW. (b) TEM image of a MoO_3-coated CdSNW. (c) HRTEM image of the u-CdSNW and its corresponding FFT pattern. (d) HRTEM image of the MoO_3-coated CdSNW and its corresponding FFT pattern.

transfer doping approach could provide an alternative doping method for other semiconductor nanostructures.

The single-crystal u-CdSNWs were fabricated by evaporation of pure CdS powder at 850 °C in a quartz tube furnace based on a typical vapor-liquid-solid mechanism, in which gold nanoparticles can direct the one-dimensional growth of NWs at high temperature.[31] After synthesis, the morphologies, phase structures and chemical compositions of the CdSNWs were studied by SEM, EDS, XRD, and XPS (see Supporting Information, Figure S1). Transmission electron microscopy (TEM) analysis in **Figure 1**(a) reveals the single crystalline nature of u-CdSNWs. A typical high-resolution TEM (HRTEM) image of the u-CdSNW in Figure 1(c) shows a lattice spacing of 0.67 nm, coinciding with the lattice spacing of (0001) planes. This preferential growth orientation along [0001] was also verified by in-situ fast Fourier transform (FFT) pattern. Figures 1(b) and 1(d) show a typical TEM and HRTEM image of a single NW after coating with MoO_3, respectively, from which the contrast between surrounding ultrathin MoO_3 film and inner u-CdSNW can be easily visualized. Furthermore, the single crystalline characteristics were well retained after surface coating.

In order to evaluate the effect of surface charge transfer doping, we fabricated two-probe single CdSNW-FETs as illustrated in **Figure 2**(a), in which Cu/Au metal was chosen as an electrode material in that it can form *ohmic* contact to the p-type CdSNW. Figure 2(b) compares the electrical conduction of pure MoO_3 thin film (~100 nm), an individual u-CdSNW with and without MoO_3 (~100 nm). It can be seen that the u-CdSNW are virtually insulating with a resistance as high as 3.3×10^{11} Ω. Interstingly, this value decreases dramatically by more than 7 orders of magnitude, to 4.7×10^3 Ω upon coating with a ~100 nm thick MoO_3 layer. Though the origin behind this phenomenon is unclear at this stage, it is at least certain that this pronounced increase in conductivity is not due to the conductance enhancement of pure MoO_3 layer whose resistivity is ~5.4×10^{10} Ω. Figure 2(c) depicts the gate-dependent source-drain current (I_{DS}) versus source-drain voltage (V_{DS}) curves of a representative MoO_3-coated (~100 nm) single CdSNW FET at varied gate voltage (V_G) ranging from –40 V to +20 V at room temperature. It is found that the conductance of the CdSNW decreases monotonously with increasing V_G, indicative of typical p-type electrical conduction behavior. It is worth pointing out that p-type CdSNW has been never achieved previously. According to the transfer characteristic curves shown in Figure 2(d), hole mobility (μ_h) and concentration (n_h) are estimated to be 2035 cm^2 V^{-1} s^{-1} and 6.1×10^{17} cm^{-3}, respectively,

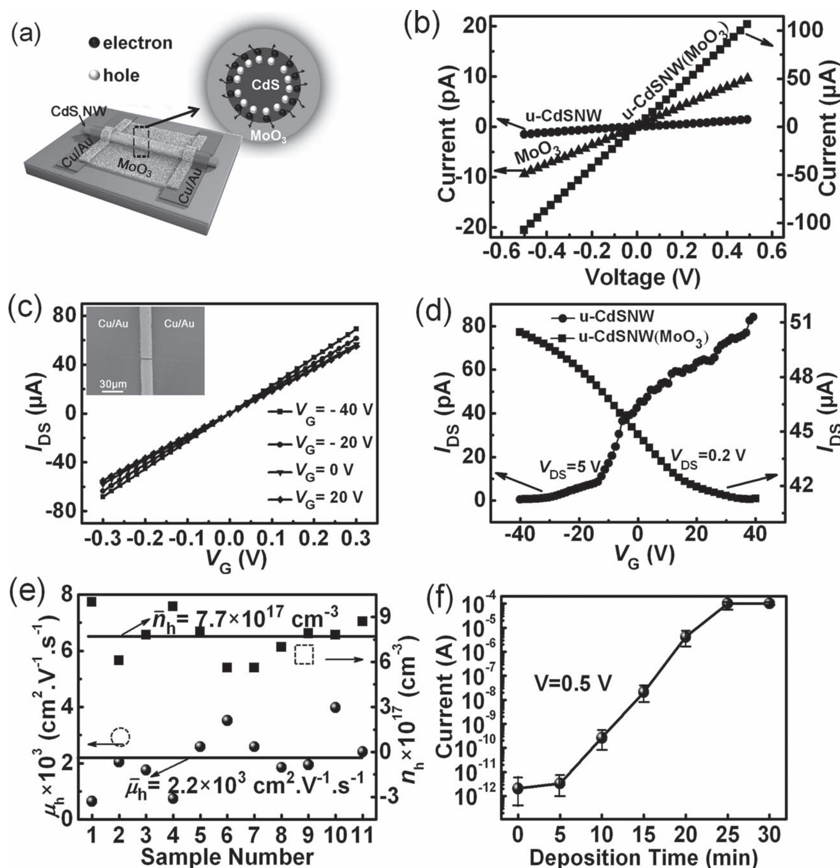

Figure 2. (a) Structural illustration of the bottom-gate FET based on single u-CdSNW after coating MoO_3, the upper inset illustrates the surface charge transfer at the CdSNW/MoO_3 interface. (b) *I–V* curves of MoO_3 layer and single u-CdSNW before and after MoO_3 film coating. (c) I_{DS}–V_{DS} characteristics of the device measured at varied V_G ranging from -40 V to 20 V at a step of 20 V. Inset shows a SEM image of the device with a channel length of 18 µm. (d) Transfer characteristics of the device before (V_{DS} = 5 V) and after (V_{DS} = 0.2 V) MoO_3 coating. (e) The statistical distribution of the hole mobility and concentration of 11 representative MoO_3-coated u-CdSNW FET. (f) The current of the MoO_3-coated CdSNW vs. deposition duration, the deposition rate was set at 4 nm/min.

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Table 2. Summary of carrier mobility, carrier concentration, resistivity of various doped CdS nanostructures and thin films.

	n/p type	μ_e/μ_h (cm^2/Vs)	n_e/n_h (cm^{-3})	ρ (Ω·cm)	Ref.
CdSNW (MoO_3)	p	~2.2×10^3	~7.7×10^{17}	~5.1×10^{-3}	Our work
u-CdSNW	n	~1.5×10^{-3}	~1.1×10^{16}	~3.6×10^5	Our work
CdS:InNR	n	~146	~2.4×10^{16}	~3.7	[13]
CdS:PNR	n	~14.8	/	/	[14]
CdS:GaNW	n	~2.1	~2.6×10^{17}	~1.0	[15]
CdS:Cu thin film	p	~1.1	~9.8×10^{19}	~29.8	[22]

in stark contrast with the weak n-type conductance of u-CdSNW (μ_e: 1.5×10^{-3} cm^2 V^{-1} s^{-1}, n_e: 1.1×10^{16} cm^{-3}) (see Supporting Information, Figure S2). As discussed later, this hole mobility, about 3 orders of magnitude higher than that of Cu doped p-type CdS film (**Table 2**), can be ascribed to the high crystallinity and clean surface of the u-CdSNW. It should be noted that this doping technique offers two characteristic advantages, which are important for various devices application: Firstly, this method was highly reproducible. We in total measured eleven NWs in order to have a statistical significance. It was found that all NWs show obvious p-type conduction behavior, with an average hole mobility and hole concentration of 2186.4 cm^2 V^{-1} s^{-1} and 7.7×10^{17} cm^{-3}, respectively. Secondly, like traditional doping method, this surface charge transfer doping technique can also allow good controllability of the electrical properties. As shown in Figure 2(f), by choosing appropriate deposition duration, i.e., the different MoO_3 layer thickness, the electrical conductance of undoped CdSNWs can be tunably modulated in a wide range of 7 orders of magnitude.

The electrical inversion from n-type to p-type conductance signifies that substantial holes were injected into the NW from MoO_3 after surface modification. As a matter of fact, this charge transfer doping is due to their distinct difference in Fermi levels. For the u-CdSNWs, the conduction band minimum (E_c) and the valence band maximum (E_v) of the CdSNWs are estimated to be −3.92 and −6.32 eV, respectively from UPS analysis (Supporting Information, Figure S3). Thereby, the Fermi level is far above that of MoO_3 with the low unoccupied molecular orbital of −6.7 eV (LUMO) and highest occupied molecular orbital −9.7 eV (HOMO), respectively.[32–34] This feature greatly facilitates the spontaneous transfer of electrons from semiconductor to surface dopants and therefore gives rise to the accumulation of huge amount of holes within CdSNWs. In fact, this surface charge transfer doping effect was experimentally corroborated by in-situ XPS analysis (see details of the sample preparation and analysis in Supporting Information). The Cd 3d and S 2p evolution with increasing thickness of MoO_3 (Supporting Information, Figures S4(a) and 4(b)). A gradual shift to low binding energy was observed when the thickness increases from 2 to 20 nm. Careful examination reveals a total shift of 0.37/0.41 eV and 0.52/0.56 eV, for Cd 3d and S 2p, respectively. This binding energy shift corresponds to the upward energy level bending from bulk to interface, suggesting that CdS accumulates holes at the u-CdS/MoO_3 interface. In fact, the accumulation of holes (loss of electrons) in u-CdSNWs is also confirmed by the Mo 3d spectra evolution in which a substantial shift of 0.78 eV towards low binding energy was observed.

The hole injection from MoO_3 film can account for the extremely high hole mobility, as often observed in the two-dimensional electron gas (2DEG).[35,36] the as-synthesized u-CdSNWs have high-quality single crystal structure without any impurity atoms. What is more, the mobile holes and MoO_3 (parent acceptor impurities) are spatially separated from each other in an irreversible manner, leading to little scattering caused by acceptor impurities which is the dominant scattering mechanism of the traditional volume doped semiconductors. As a result, the mean free path of the mobile hole is substantially increased. Thus the hole mobility of MoO_3-coated CdSNWs may greatly exceed that of other impurity atoms doped CdS nanostructures.

Figure 3(a) depicts the conductivity variation of surface doped CdSNW corresponding to increasing temperature. Clearly, the conductivity of MoO_3-coated CdS nanowires is observed to decrease at first in the temperature range from 8 to 160 K. With the temperature further increased, on contrary, it begins to increase slowly. As we will discuss later, as a result of the distinctive hole mobility and concentration evolution at low temperature, this "V" shape temperature-dependent electrical characteristic is completely different from that of traditionally doped semiconductors whose conductivities normally decrease monotonically with decreasing temperature by more than 1–3 orders of magnitude.[37,38] Figure 3(c) shows the hole mobility and concentration of MoO_3-coated CdSNWs as a function of temperature. Basically, it was seen that the hole mobility decreases with increasing temperature, with a rate of change less than 1 order of magnitude. This phenomenon is possibly associated with suppression of scattering of acoustic phonons, due to the reduced phase space for backscattering in the one-dimensional (1D) nanostructure.[39,40] With regard to the hole concentration, on contrary, it increases with increasing temperature, in consistence with what is found in 2DEG.[36] This result is understandable simply because at higher temperature, more electrons within the CdSNW will have sufficient energy to overcome the established barrier between CdSNW and MoO_3 and move to MoO_3 layer. Consequently, the hole concentration of the MoO_3-coated CdSNW will increase when new equilibrium was achieved. It should be noted that the surface doped NW also shows outstanding electrical stability in ambient condition. As can be seen in Figure 3(d), after storage in air for two months, the conductivity of a MoO_3-coated CdSNW remains almost identical. Without question, this good stability and aforementioned excellent electrical property at low temperature will greatly facilitate its applications in low-temperature nano-electronic devices.

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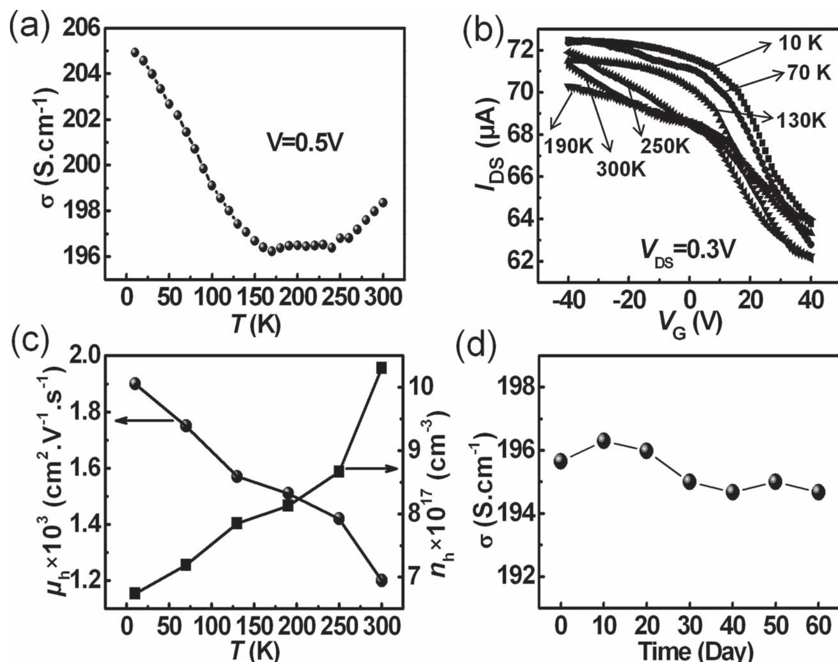

Figure 3. (a) The conductivity of single MoO_3-coated CdSNW at a fixed voltage of 0.5 V as a function of temperature. (b) I_{DS}-V_G curves of the MoO_3-coated CdSNW based FET device (V_{DS} = 0.3 V) at different temperatures. (c) Temperature dependent hole mobility and concentration of MoO_3-coated CdSNWs. (d) Conductivity evolution of the MoO_3-coated CdSNW as a function of time.

We note that the surface charge transfer doping is so effective that even heavily Ga-doped n-type CdSNW could be completely converted to p-type as well. **Figure 4**(a) and Figure S5 compared the transport properties of the n-type CdS:GaNWs with and without MoO_3 film deposition, from which, one can see that the huge amount of electrons (7.1×10^{17} cm^{-3}) gave way to holes (1.8×10^{17} cm^{-3}) upon surface doping. Meanwhile, carrier mobility changed from 98.2 cm^2/Vs (μ_e) to 14.8 cm^2/Vs (μ_h). Note that due to the strong scattering effect of Ga atoms in the NWs, the hole mobility of the Ga-doped CdSNW FET is much lower than that of u-CdSNW after MoO_3 layer coating. By taking advantage of this phenomenon, we were able to fabricate nano p-n homojunction through selective deposition of the MoO_3 layer on half part of the n-type Ga-doped CdSNW. Figure 4(b) plots a typical *I–V* curve of the as-fabricated homojunction, which displays pronounced rectifying behavior with a low turn-on voltage at a forward bias of ~1 V. The on/off current ratio is ~1.6×10^2 when the voltage changes from +2 to −2 V. This rectifying behavior can be exclusively attributed to the junction formed by partial deposition of MoO_3 layer considering the fact that ohmic contacts were formed at both Cu/Au/Ga-doped CdSNW and In/Ga-doped CdSNW interfaces, as shown in the inset of Figure 4(b). The ideality factor n for this nano p-n junction can be expressed as: $n = (q / K_B T) dV/d\ln I$, where K_B and T are the Boltzmann constant and the temperature in kelvins, respectively. By choosing the low-bias zone (0.1–0.4 V), an ideality factor of 2.8 was obtained. Remarkably, the as-fabricated p-n junction can function as efficient photovoltaic device to harvest solar light. Figure 4(c) shows the *I–V* curves of the homojunction diode under while light illumination (~1.5 mW·cm^{-2}). The cell gave an open circuit photovoltage (V_{OC}) of 0.10 V, a short circuit current density (J_{SC}) of 0.72 mA/cm^2, and a fill factor (*FF*) of 35.23%, yielding a power conversion efficiency (η) of 1.65%, comparable to that of other single semiconductor nanostructures based photovoltaic devices.[41,42] The working mechanism of such CdSNW homojunction solar cell can be interpreted in terms of the energy band diagram shown in Figure 4(d). Under light illumination, photons with energy larger than the band gap of CdSNWs were absorbed by the device, and the photogenerated electron-hole pairs will be separated by the built-in potential at the depletion region. The resulted free electrons and holes will drift towards opposite directions, and therefore form the photocurrent in external circuit.

In summary, we report a novel surface doping technique, via which p-type CdSNWs can be readily prepared without the introduction of foreign atoms into the CdSNW lattice. Electrical

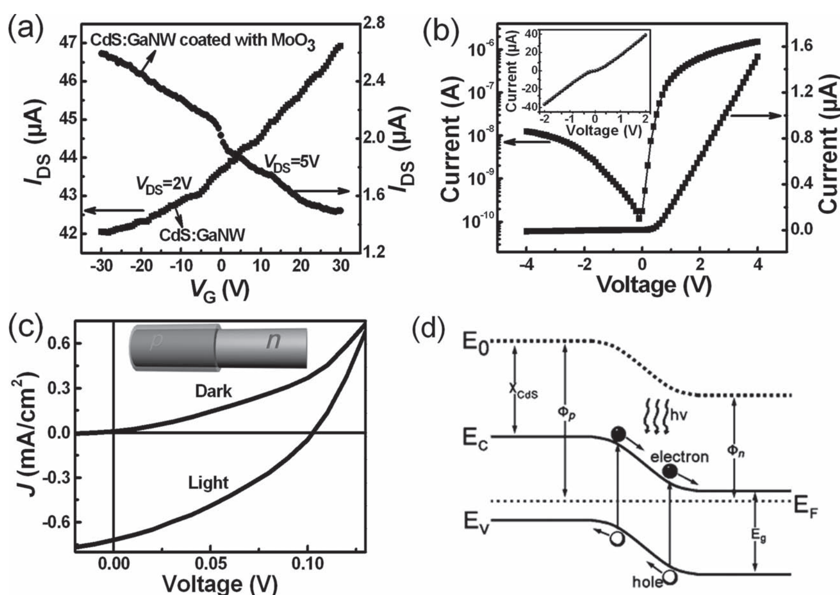

Figure 4. I_{DS}-V_G characteristics of Ga-doped CdSNW bottom-gate FET before (V_{DS} = 2 V) and after (V_{DS} = 5 V) MoO_3 coating. (b) Rectifcation characteristics of the homojunction based on single CdSNW measured in the dark, the inset shows the *I–V* plots of a Ga-doped CdSNW without MoO_3. (c) Photovoltaic characteristics of the single CdSNW homojunction. (d) Energy band diagram of CdSNW homojunction photovoltaic device under light illumination.

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measurements reveal an obvious p-type conductance of the CdSNWs after coating with MoO_3 thin layer, with an average hole mobility and concentration of 2035 $cm^2/V \cdot s$ and 7.7×10^{17} cm^{-3}, respectively. By in situ XPS analysis of CdSNWs as a function of increasing MoO_3 coverage, we found that a considerable quantity of electrons was transferred spontaneously from CdSNWs to MoO_3 layer due to the distinct difference in Fermi levels. By partially coating an individual CdSNW, excellent rectifying p-n nano-junction diode with a high on/off current ratio of ~1.6×10^2 and a low forward turn-on voltage of about 1.0 V at room temperature can be fabricated. Under light illumination, the p-n homojunction diode showed obvious photovoltaic behavior with a power conversion efficiency (η) up to 1.65%. This study proves that this surface charge transfer scheme by surface modification has great potential applications for fabrication of semiconductor nanostructures based devices in the future.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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