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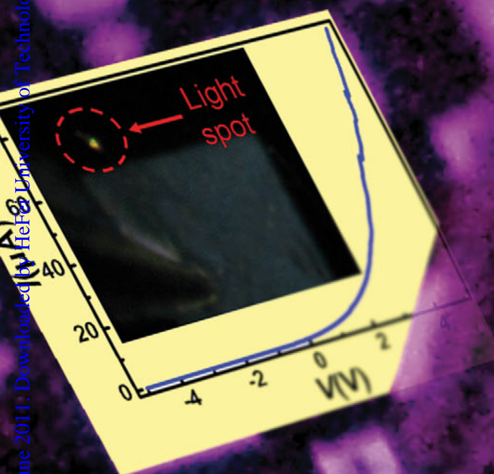

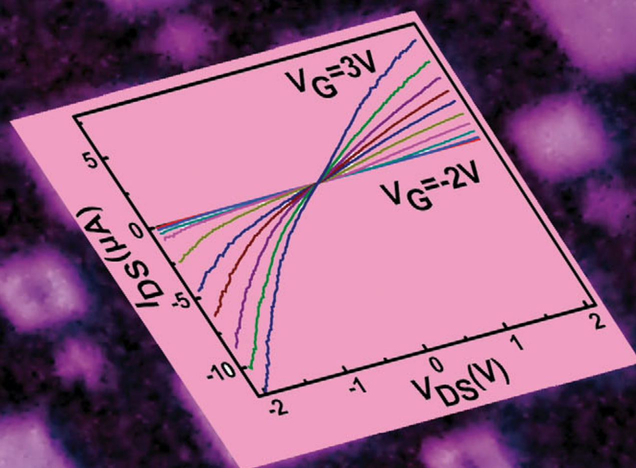

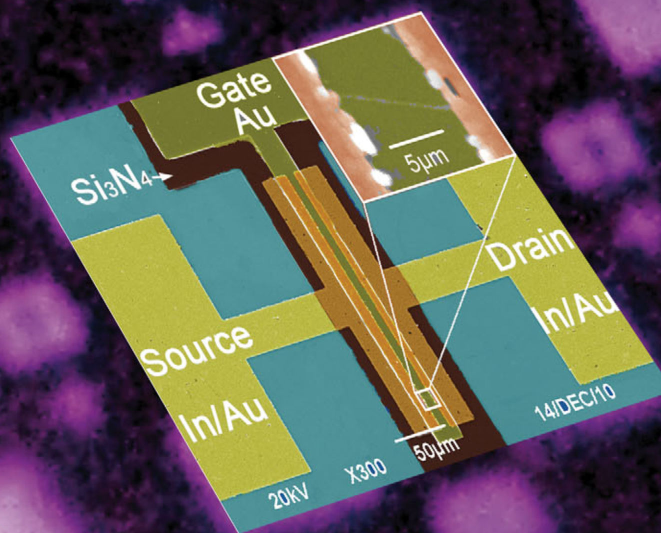

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PAPER

Tuning the electrical transport properties of n-type CdS nanowires *via* Ga doping and their nano-optoelectronic applications

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Gallium-doped n-type CdS nanowires (NWs) were successfully synthesized *via* a thermal evaporation method. The conductivities of the CdS NWs were dramatically improved by nearly nine orders of magnitude after Ga doping, and could be further tuned over a wide range by adjusting the doping level. High-performance metal–insulator–semiconductor field-effect transistors (MISFETs) were constructed based on the single CdS : Ga NW with high-κ Si_3N_4 dielectrics and top-gate geometries. In contrast to back-gate FETs, the MISFETs revealed a substantial improvement in device performance. Nano-light emitting diodes (nanoLEDs) were fabricated from the CdS : Ga NWs by using a n-NW/p^+-Si substrate hybrid device structure. The nanoLEDs showed a bright yellow emission at a low forward bias. It is expected that the Ga-doped CdS NWs with controlled electrical transport properties will have important applications in nano-optoelectronic devices.

I. Introduction

CdS is an important II–VI semiconductor, with a wide direct band-gap of 2.42 eV at room temperature. It has attracted increasing interest owing to its unique electrical and optoelectronic properties. In the past decade, many efforts have been made to fabricate CdS nanostructures and further exploit their potential applications in new-generation nanoelectronics and nano-optoelectronics.[1,2] A variety of nanodevices, including metal–oxide–semiconductor field-effect transistors (MOSFETs),[3–5] optoelectronic switches,[6,7] sensors,[8,9] waveguides,[10,11] electro-optic modulators,[12] light-emitting diodes (LEDs),[13] and lasers *etc.*, have been actualized based on CdS nanostructures.

Doping is vital to the use of the semiconductor nanostructures in electronic and optoelectronic devices. Through appropriate n- and p-type doping, the electrical transport properties of the nanostructures could be efficiently tuned, facilitating the device construction and thereby promoting their practical applications. Therefore, it has been an urgent task in nanodevice research to survey, both theoretically and experimentally, the capability for achieving efficient doping in semiconductor nanostructures. As for CdS nanostructures, they are highly insulating, in the case of those without doping, due to the high crystal quality and the little amount of nonstoichiometric defects. Although the growth and optical properties of CdS nanostructures have been intensively studied over the past decade,[14,15] controlled doping of them is seldom reported and remains a challenging issue.[16] On the other hand, the applications of CdS nanostructures with controlled doping in high-performance nanoelectronic and nano-optoelectronic devices needs to be further exploited.

Herein, we demonstrate efficient n-type doping in CdS nanowires (NWs) by using gallium (Ga) as the donor element *via* thermal evaporation. The conductivities of the CdS NWs are dramatically enhanced through Ga doping and could be rationally tuned over a wide range by adjusting the doping level. High-performance nanoFETs and nanoLEDs are constructed based on the Ga-doped CdS NWs, indicating promising applications of the doped CdS nanostructures in future nanoelectronics and nano-optoelectronics.

II. Experimental details

The synthesis of the Ga-doped CdS NWs was conducted in a horizontal tube furnace *via* a simple thermal evaporation method. A similar method has been used for the synthesis of chlorine-doped CdS NWs and indium-doped CdSe NWs in our previous works.[7,17] In this experiment, a mixed powder of CdS (Aldrich 99.99%), Ga, and Ga_2O_3 (0.5 g) was used as the evaporation source and placed at the center region of the furnace. The molar ratio of Ga : Ga_2O_3 in the evaporation

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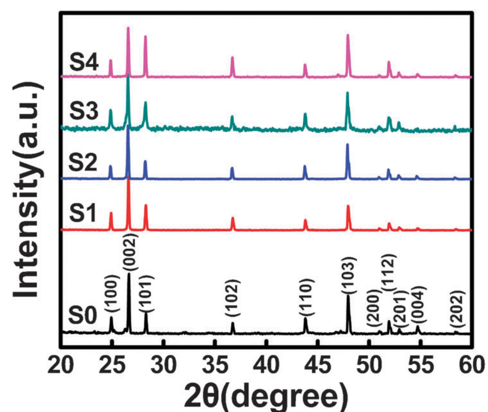
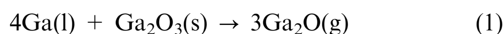
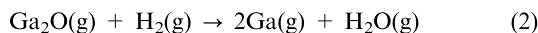


Fig. 1 XRD patterns of both the intrinsic CdS NWs (S0) and the CdS : Ga NWs with increasing doping levels from S1 to S4.

source is 4 : 1, allowing the generation of Ga vapor *via* the following reactions:



$$4Ga(l) + Ga_2O_3(s) \rightarrow 3Ga_2O(g) \quad (1)$$



$$Ga_2O(g) + H_2(g) \rightarrow 2Ga(g) + H_2O(g) \quad (2)$$

It is noted that our primary attempt to use the element Ga as the n-type dopant was demonstrated to be unsuccessful since the element Ga has a very high boiling point. Si substrates coated with 10 nm Au catalyst were placed downstream, ~10 cm from the evaporation source. During the experiments, a constant H_2 (5% in Ar) gas flow of 60 sccm was fed and the pressure in the tube was adjusted to 200 Torr. The evaporation source was heated to 880 °C and maintained at that temperature for 2 h. In this work, four samples with varied Ga doping levels were synthesized and marked as S1, S2, S3, and S4, corresponding to the increased Ga and Ga_2O_3 mixture to CdS mass ratio of 1%, 2%, 4%, 8%, respectively. Undoped CdS NWs were also synthesized under the same conditions, except for the use of the Ga dopant, for comparison and marked as S0.

The structures and morphologies of the as-synthesized products were characterized by X-ray diffraction (XRD, Rigaku D/Max-γ B, with Cu-Kα radiation), field-emission scanning electron microscopy (FESEM, Philips XL 30 FEG), and high-resolution transmission electron microscopy (HRTEM, JEOL-2010). The compositions of the products were detected by energy-dispersive X-ray spectroscopy (EDX, attached to the SEM) and X-ray photoelectron spectroscopy (XPS, VGESCALAB MKII). Room-temperature photoluminescence (PL) spectra were measured using a 325 nm He–Cd laser as the excitation source (LABRAM-HR).

To assess the electrical transport properties of the CdS : Ga NWs, two types of FETs, including the back-gate MOSFETs and the top-gate metal–insulator–semiconductor FETs (MISFETs), were constructed based on the individual CdS NWs. As for the former, the as-synthesized CdS NWs were first dispersed on a SiO_2 (300 nm)/p^+-Si substrate, followed by photolithography and lift-off processes to define In (200 nm)/Au (20 nm) source and drain electrodes on the NWs. The degenerately doped Si substrate then served as the global back gate. To fabricate the top-gate MISFETs, a thin layer of Si_3N_4 (100 nm) gate dielectric was deposited by magnetron sputtering, and then an Au (40 nm) gate electrode was fabricated *via* electron beam evaporation. To construct the nanoLEDs, a hybrid device structure that consisted of the n-CdS NW and the p^+-Si substrate was used (Fig. 6a). The SiO_2/p^+-Si substrate was first etched with dilute HF (5%) solution to obtain the square SiO_2 insulator islands on the p^+-Si substrate, and then the CdS : Ga NWs were dispersed on the substrate. P–n junctions were formed at the regions where the NWs contacted with the p^+-Si substrate. Subsequently, In electrodes were formed on the SiO_2 insulator pads, covering the other ends of the NWs. All of the electrical measurements were conducted at room temperature in the dark by using a semiconductor characterization system (Keithley 4200-SCS).

III. Results and discussion

Fig. 1 depicts the XRD patterns of the samples, in which all of the diffraction peaks could be assigned to wurtzite CdS (JCPDS 41-1049) and no impurity peaks were observed, indicating the high phase purity of the products. In addition, the diffraction peaks of the Ga-doped CdS NWs do not show obvious peak broadening or peak shift compared with the undoped CdS NWs, implying that the doping has little influence on the crystal quality of the NWs.

Fig. 2(a) shows a typical SEM image of the CdS : Ga NWs. The NW surfaces are clean and smooth and free of visible particles and impurities, except for the existence of Au catalyst tips. The NWs have diameters in the range of 50–200 nm and lengths from several tens of micrometres up to hundreds of micrometres. The inset in Fig. 2(a) depicts the EDX spectrum of the CdS : Ga NWs, indicating that the product is composed of Cd and S elements with a molar ratio of ~48 : 52. From the HRTEM image and the corresponding fast Fourier transform (FFT) pattern (Fig. 2b), it is seen that the NWs have single

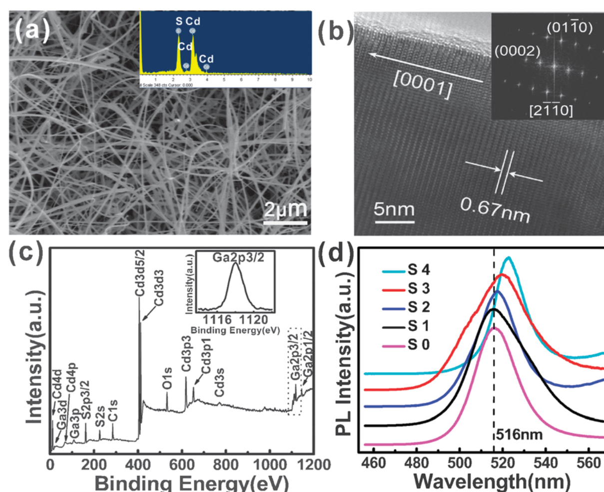


Fig. 2 (a) A typical SEM image of the CdS : Ga NWs. The inset shows the EDX spectrum. (b) A typical HRTEM image of the CdS : Ga NWs. The inset shows the corresponding FFT pattern. (c) An XPS spectrum of the CdS : Ga NWs. The inset shows the enlarged Ga 2p3/2 peak. (d) Room-temperature PL spectra of both the Ga-doped and undoped CdS NWs. The PL spectra were normalized and shifted upwards for comparison.

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crystal wurtzite structures with [0001] growth orientation. XPS measurements were performed to further detect the compositions of the CdS : Ga NWs (sample S3), as shown in Fig. 2c. In addition to the Cd and S peaks, a peak at 1118 eV that corresponds to the Ga2p3/2 core level has appeared, revealing the successful incorporation of Ga in the CdS NWs. The overall content of Ga in this sample is estimated to be ~1.9 at.%. We note that a evident red-shift of the emission bands is observed in the PL spectra of the samples (Fig. 2d). The emission band of the undoped CdS NWs (S0) is centered at 516 nm, which corresponds to the near band-edge (NBE) emission of CdS, while the bands shift remarkably to longer wavelengths of 516.1 nm, 517.5 nm, 519.5 nm, and 522.8 nm for S1, S2, S3, and S4, respectively. The red-shift of the emission bands reflects the narrowing of the CdS NW band-gap, which is caused by the broadening of the conduction band due to the introduction of a Ga donor level.[18] Therefore, the PL spectra also provide clear evidence for the successful Ga doping in the CdS NWs.

Fig. 3a shows the typical *I–V* curves of the Ga-doped CdS NWs measured by a two-probe method. The linear shape of the *I–V* curves indicates the ideal ohmic contact of the In electrodes with the NWs. We note that the conductance of the CdS : Ga NWs is dramatically increased compared with the undoped one (inset in Fig. 3a). The resistance of the undoped CdS NW is as high as 2.5×10^7 MΩ, while it decreases to 5.3×10^2, 11, 0.88, and 0.13 MΩ for S1, S2, S3, and S4, respectively, with the increasing level of Ga doping. To gain statistical significance, the conductivities of 30 NWs for each sample were measured and the corresponding conductivity histogram is depicted in Fig. 3b. Significantly, the conductivity of the CdS NWs could be tuned over a wide range of about nine orders of magnitude from 10^{-7}–10^{-6} S cm^{-1} for S0 to 5×10^{-3}–1×10^{-1} S cm^{-1} for S1, 0.1–5 S cm^{-1} for S2, 5–100 S cm^{-1} for S3, and 10–500 S cm^{-1} for S4. The remarkable increase in the conductivity is a result of the Ga doping in the CdS NWs, demonstrating that Ga could be a very efficient donor dopant to tune the electrical transport properties of the CdS NWs.

Fig. 4a shows a schematic illustration of the back-gate MOSFET based on the individual CdS : Ga NWs. From the typical gate-dependent source–drain current (I_{DS}) *versus* source–drain voltage (V_{DS}) curves of the CdS : Ga NW (sample S3) (Fig. 4b), it is seen that the conductance of the NW increases (decreases) consistently with the increasing (decreasing) gate voltage (V_G), revealing the n-type nature of the CdS : Ga NW. This result is consistent with the anticipation that excess electrons will be generated when the Cd^{2+} ions are substituted by the Ga^{3+} ions. The field-effect electron mobility (μ_e) of the CdS : Ga NW could be estimated to be ~2.1 cm^2 V^{-1} s^{-1} based on the equation:[19]

$$\mu_e = Lg_m \ln(4h/d)/2\pi\varepsilon\varepsilon_{SiO_2}V_{DS} \quad (3)$$

where g_m = 2.3 nS represents the transconductance of the nanoFET and can be deduced from the slope of the I_{DS}–V_G

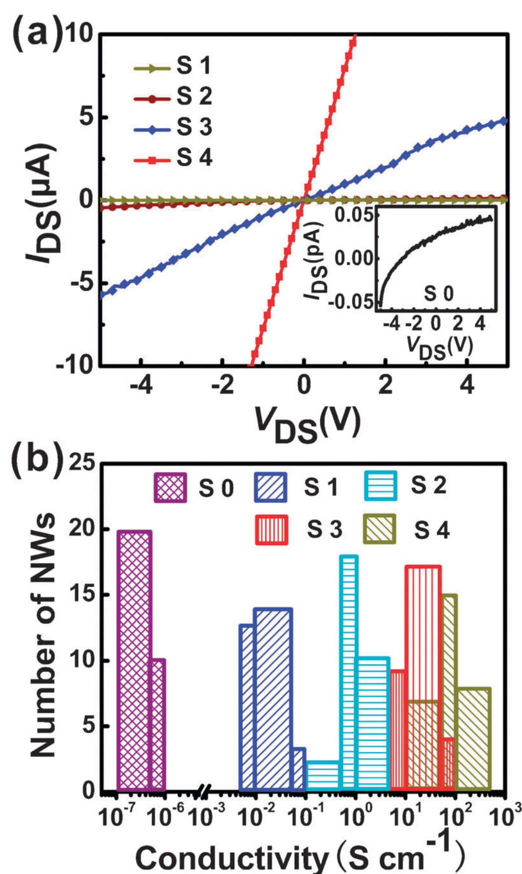

Fig. 3 (a) Typical *I–V* curves of the CdS NWs with varied doping levels in the dark. The inset shows the *I–V* curve of an undoped CdS NW for comparison. (b) A conductivity histogram for the samples. 30 NWs each for S0, S1, S2 S3 and S4 were measured in dark.

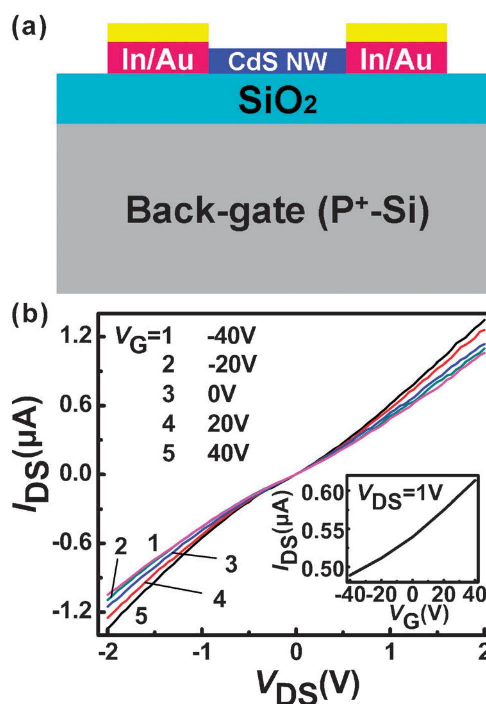

Fig. 4 (a) A schematic illustration of the back-gate CdS NW MOSFET. (b) I_{DS}–V_{DS} curves of the CdS : Ga NW (S3) measured at varied V_G. V_G increases from −40 to 40 V in steps of +20 V. The inset shows the I_{DS}–V_G curve at V_{DS} = +1 V.

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curve in the linear region (inset in Fig. 4b) according to the relationship of $g_m = dI_{DS}/dV_G$. L, h, d, and ε_{SiO_2} represent the NW channel length (~8 μm), SiO_2 dielectric layer thickness (300 nm), NW diameter (~100 nm), and the SiO_2 dielectric constant (3.9), respectively. Although the back-gate CdS : Ga NW FET exhibits an obvious gating effect, its overall device performance is still very poor, such as the large operation voltage, small I_{on}/I_{off} ratio (1.3 for V_G at ±40 V), and low electron mobility. It is suggested that the weak gate coupling caused by the thick dielectric and the back-gate device configuration is responsible for its poor performance.[4,19]

To further improve the device performance, top-gate MISFETs were fabricated based on the CdS : Ga NWs (sample S3) by using high-κ Si_3N_4 ($\varepsilon \sim 7.5$) instead of the SiO_2 dielectric. Fig. 5a and b depict the SEM image and the schematic illustration of the device, respectively. Significantly, the top-gate MISFET exhibits a remarkable improvement in the device performance. The device could be switched between the accumulation state and the depletion state within a small gate voltage range from −2 V to +3 V (Fig. 5c). From the transfer characteristics of the device (Fig. 5d), the I_{on}/I_{off} ratio of the device is as high as $\sim 10^7$ in the applied gate voltage range. The g_m value of the device further increases to 1.07 μS at V_{DS} = 1 V, while the threshold voltage (V_{th}) decreases to −0.3 V. The field-effect mobility of the device is estimated to be 241.6 $cm^2\ V^{-1}\ s^{-1}$ according to the following equation:[19]

$$\mu_e = Lg_m \ln(1 + 2h/d)/2\pi\varepsilon\varepsilon_{Si_3N_4}V_{DS} \quad (4)$$

where $\varepsilon_{Si_3N_4}$ is the dielectric constant of Si_3N_4. On the other hand, subthreshold swing (S) is also an important parameter for a FET, which is defined as $S = dV_G/d\log_{10}I_{DS}$ in the subthreshold region. A small S value is desired to efficiently switch off (on) a FET within a small voltage range. Here, S is deduced to be 114 mV dec^{-1} for the top-gate CdS : Ga NW MISFET, in contrast to the much larger value (~816 V dec^{-1}) for the back-gate FET, and approaches the theoretical value (60 mV dec^{-1}) for a FET at room-temperature. Moreover, the electron concentration (n) in the CdS : Ga NW is determined to be 2.6 × 10^{17} cm^{-3} from the equation $n = \sigma/e\mu_e$, where σ is the conductivity of the NW at zero gate voltage, and e is the elementary charge. This value is smaller than that obtained from the XPS detection (~1.9 at.%, corresponding to a Ga donor concentration $>10^{19}$ cm^{-3}). Since the XPS signal is detected from a large area of NW film, the uneven doping and the existence of a small amount of Ga impurities will result in the large XPS value. On the other hand, this result also indicates that only a small portion of Ga donors could be activated and contribute to the conductivity of the CdS : Ga NWs. It is noted that over ten CdS : Ga NW MISFETs were measured in this work. All of them show stable device performances with mobilities larger than 200 $cm^2\ V^{-1}\ s^{-1}$ and S in the range of 80–150 mV dec^{-1}, indicating good reproducibility of the devices.

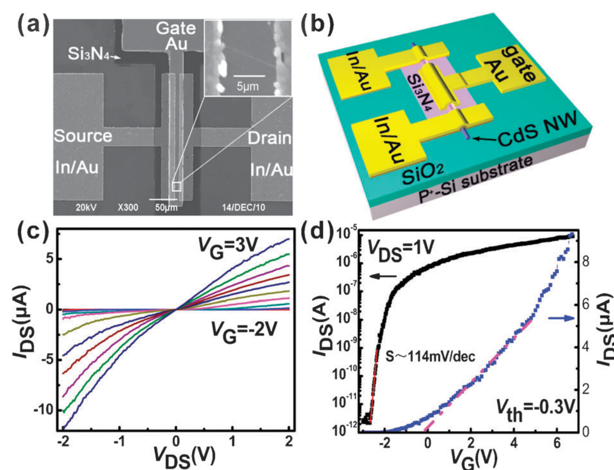

Fig. 5 (a) A SEM image of a representative top-gate CdS NW MISFET. The inset shows an enlarged SEM image of the FET channel. (b) A schematic illustration of the top-gate CdS NW FET. (c) I_{DS}–V_{DS} curves measured at varied V_G. V_G increases from −2 to +3 V in steps of +0.5 V. (d) A I_{DS}–V_G curve measured at V_{DS} = +1 V. Both the subthreshold region and the liner part of the I_{DS}–V_G curve were fitted by straight lines to obtain the values of subthreshold swing and transconductance.

The substantial improvement in the device performance of the top-gate CdS : Ga NW MISFET could be attributed to the use of the high-κ Si_3N_4 dielectric as well as the top-gate device configuration.[4,5,19] The thin Si_3N_4 insulator leads to a remarkable enhancement in the channel capacitance and thus allows more efficient gate modulation to the conduction channel. This gate modulation is further improved by the surrounding top gate. We also note that nanoFETs fabricated from the undoped CdS NWs (S0) show very poor performances with faint gating effects even when the same top-gate geometry and the high-κ dielectric are used (data not shown), indicating that the appropriate channel doping plays an important role in obtaining high-performance nanoFETs. A serious contact problem in nanoFETs fabricated from intrinsic nanostructures usually causes the degeneration of the device performance. By increasing the carrier concentration in the conduction channel, the contact barrier, if it exists, will be much lower and thinner, thus allowing the carriers to pass through the interface *via* direct electron tuning and resulting in a low contact resistance. Besides the electrode contact, the channel doping also offers the capability to control the threshold voltage, which is important for the practical application of the nanoFETs. However, the highly doped CdS NWs show worse performances, since the NWs become more metallic rather than semiconducting in this case. Therefore, a balance should be taken between the doping concentration and the device performance. In this work, sample S3, which has a modest doping concentration, is found to be most suitable for high-performance device applications.

To demonstrate the promising applications of the n-type CdS : Ga NWs in nano-optoelectronics, nanoLEDs based on the NWs were also constructed, as shown in Fig. 6a. The n-CdS NW/p^+-Si substrate hybrid p–n junction exhibits excellent rectification behavior with a small turn-on voltage of ~2.4 V (Fig. 6b). A bright yellow spot of light could clearly be observed by the naked eye from the optical microscope in the probe station even at a relatively low forward bias of +5 V (inset in Fig. 6b), and the light intensity could be further adjusted by changing the forward voltage.

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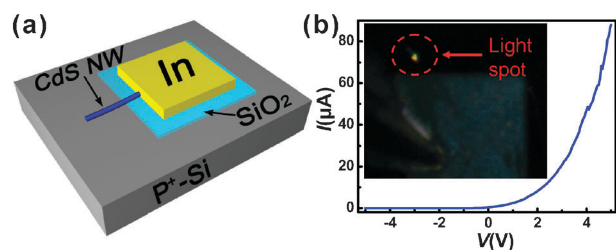

Fig. 6 (a) A schematic illustration of the nanoLED fabricated from the n-CdS NW/p$^+$-Si substrate heterojunction. (b) The rectifying characteristic of the hybrid p–n junction. The inset shows the yellow spot of light captured by the optical microscopy on the probe station.

IV. Conclusions

In summary, Ga-doped CdS NWs were successfully synthesized by using a Ga_2O_3 and Ga mixed powder as the n-type dopant *via* thermal evaporation. Through adjusting the Ga doping level, the conductivities of the CdS : Ga NWs could be tuned over a wide range of nearly nine orders of magnitude. High-performance MISFETs based on individual NWs were constructed by using a high-κ Si_3N_4 dielectric and a top-gate device geometry, and showed a substantial improvement in device performance. Moreover, nanoLEDs were obtained by taking advantage of a n-CdS NW/p$^+$-Si substrate hybrid device structure. Bright yellow emission from the nanoLED was clearly observed at a relatively low forward voltage. It is expected that the CdS NWs with tunable transport properties have great potential in nanoelectronic and nano-optoelectronic devices.

Acknowledgements

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