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Nonvolatile multibit Schottky memory based on single n-type Ga doped CdSe nanowires

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Abstract
Nonvolatile resistive switching has been observed for the first time in CdSe nanowire (NW)/Au Schottky barrier diodes, where a Schottky contact electrode and an Ohmic contact electrode were formed at the Au/CdSe NW and CdSe NW/In interfaces, respectively. The CdSe NWs Schottky devices were found to possess multibit storage ability in an individual nanowire, and exhibited excellent memory characteristics, with a resistance on/off ratio exceeding four orders of magnitude, a long retention time of over 10^4 s and a lower operating voltage of 2 V. By replacing the SiO_2/Si substrate with a poly ethylene terephthalate substrate, flexible and transparent memory devices with superior stability under strain were realized. The resistive switching of CdSe NW/Au Schottky devices is understood by electron trapping and detrapping in the interfacial oxide layer. Our findings provide a viable way to create new functional high-density nonvolatile multibit memory devices compatible with simple processing techniques for normal one-dimensional nanomaterials.

(Some figures may appear in colour only in the online journal)

1. Introduction

The resistive switching (RS) effect, in which the resistance can be reversibly switched by an external electrical field, has attracted increasing attention due to its potential application for nonvolatile memory devices [1–4]. RS memory has been considered as next-generation high-density nonvolatile memory because of its structural simplicity and excellent memory characteristics. Numerous efforts have been devoted to the construction of high-performance RS memory devices from one-dimensional (1D) nanostructures. 1D nanostructure based RS memory devices not only offer the capability of reducing the size of the memory cells beyond the limitation of current lithographic length scales but also provide a platform for exploring the underlying nanoscale RS mechanisms. Compared to conventional three-terminal field-effect transistor (FET) memory and thin film based memory, two-terminal 1D nanostructure based RS memory devices have the great advantages of a simple fabrication process, lower power consumption, fast write/read speed and high-density storage [1, 2]. The RS phenomena previously reported have mainly focused on various oxide materials including NiO nanowire (NW) [1, 3], ZnO NW [5, 6], CoO NW [2, 7], TiO_2 [8, 9] and perovskite oxide materials [10–12]. These reported RS memory devices can be divided into three types, namely bipolar [11], unipolar [13] and threshold switching [14]. In these metal/oxide structures, the physical mechanisms for the memory are attributed to the formation of an oxygen vacancy (V_O) chain conductive filament

and electrical field-induced breakdown without forming a conductive filament [1, 3, 15–17]. In addition, some interface-related models, such as pulse-generated crystalline defects, field-induced electrochemical migration and charge-trapping-induced alteration of Schottky-like barriers, have also been reported to explain the interface-related RS effects of perovskite oxide materials [5, 18–20]. In spite of this progress, the underlying physical mechanism, especially at the nanoscale, is still a controversial issue. In the above RS memory devices, it is difficult to realize the scale-down of multibit storage to the size of a single memory cell due to the geometric configuration of these devices. Additionally, the high operating voltage limits the applications of such RS memory devices in integrated circuits. For extended RS memory functionality, the evaluation of a new type of device structure and semiconductor nanomaterial is worthy of exploration. The reported Schottky barrier diodes (SBDs) based on II–VI group nanostructure semiconductors were found to have potential applications in many nanoelectronic areas, such as logic circuits [21, 22], photodetectors [23, 24], photovoltaic devices [25, 26], and so on. Theoretically speaking, nanoSBDs of II–VI semiconductors with the resistive switching effect could be used as nonvolatile memory with expected behaviors.

In this paper, we demonstrate a two-terminal nonvolatile multibit RS memory based on Au/CdSe NW/In structure, where a Schottky contact and an Ohmic contact are formed. The CdSe NWs, which had a naturally formed ultrathin native oxide layer that served as the storage medium for the memory, were synthesized via a simple thermal evaporation method. The CdSe/Au Schottky memory devices exhibited excellent memory characteristics including high-resistance on/off ratio, long retention time and lower operating voltage. Multibit storage ability was also obtained by integrating several nanoSBDs on an individual CdSe NW. Moreover, the simple structure and fabrication process allow the memory to be easily constructed on flexible and transparent substrate while keeping a stable and robust performance. This simple and effective method for fabricating RS memory devices could also be easily extended to other one-dimensional (1D) semiconductor nanostructures.

2. Experimental details

The Ga doped CdSe NWs employed in this work were synthesized by using CdSe powder (99.99%, Aldrich) and Ga/Ga_2O_3 mixed powder as the source material and the n-type dopant, respectively, via a co-thermal evaporation method in a horizontal tube furnace [27]. Although the melting point of elementary gallium is very low, its boiling point is too high (~2100 °C) for it to be evaporated. Hence, Ga and Ga_2O_3 mixed powder was used as the dopant source in this work. Ga vapor could be generated through the following reactions at relatively low temperature (>600 °C):

$$4Ga(l) + Ga_2O_3(s) \rightarrow 3Ga_2O(g), \quad (1)$$

$$Ga_2O(g) + H_2(g) \rightarrow 2Ga(g) + H_2O(g). \quad (2)$$

In detail, about 0.2 g of CdSe and Ga and Ga_2O_3 mixed powder was loaded onto an alumina boat and transferred to the central region of the tube furnace. The content of Ga and Ga_2O_3 in the evaporation source was 8 wt% and the molar ratio of $Ga:Ga_2O_3$ was 4:1. Si substrates coated with 10 nm of gold catalyst were then placed in the downstream position about 10 cm away from the evaporation source. Before heating, the system was evacuated to a base pressure of 10^{-5} Torr, and back filled with an Ar and H_2 (5%) gas mixture with a constant flow rate of 100 sccm to a stable pressure of 150 Torr. Afterwards, the mixed powder was heated up to 890 °C and maintained at that temperature for 2 h. A layer of black wool-like product could be observed on the Si substrate surfaces after the reaction. The morphology and structure of the as-synthesized CdSe:Ga NWs were characterized by x-ray diffraction (XRD, D/max-γB), field-emission scanning electron microscopy (FESEM, SIRION 200 FEG) and high-resolution transmission electron microscopy (HRTEM, JEOL JEM-2010, at 200 kV). The composition of the CdSe:Ga NWs was analyzed by x-ray photoelectron spectroscopy (XPS, Thermo ESCALAB 250).

To construct Schottky junction devices, the as-synthesized CdSe:Ga NWs were dispersed in a parallel arrangement on a SiO_2 (300 nm)/p^+–Si substrate by a contact print technique [28], and then photolithography followed by a lift-off process was used to define indium (In, 100 nm) Ohmic contact electrodes on the NWs. Afterwards, the Au (100 nm) Schottky electrodes on the other side were defined by additional photolithography and lift-off processes. Figures 2(a) and (b) show a schematic illustration and an SEM image of the CdSe NW/Au Schottky devices. The multibit memory devices and flexible memory devices were fabricated by the same process. Electrical measurements were conducted at room temperature by using a semiconductor characterization system (Keithley 4200-SCS).

3. Results and discussion

Figure 1(a) shows a typical FESEM image of the as-synthesized CdSe:Ga NWs. The diameter and length of the NWs are in the range of 50–150 nm and 50–200 μm, respectively. The high-resolution transmission electron microscopy (HRTEM) image and the corresponding selected-area electron diffraction (SAED) pattern reveal that the NWs have a single-crystal wurtzite structure with a growth orientation of [0002] (figure 1(b)). In the x-ray diffraction (XRD) patterns (figure 1(c)), all the diffraction peaks can be assigned to wurtzite CdSe (JCPDS No. 77-2307) and no impurity phases are detected, suggesting a high phase purity of the product. X-ray photoelectron spectroscopy (XPS) measurements were performed to further detect the composition of the CdSe:Ga NWs, as shown in figure 1(d). In addition to the Cd and Se peaks, a peak appeared at ~1117 eV, that corresponded to the Ga 2p3/2 core level, revealing the successful incorporation of Ga in the CdSe NWs with an estimated Ga content of ~2.8 at.%.

Figures 2(a) and (b) show a schematic illustration and an SEM image of the CdSe:Ga NW/Au Schottky

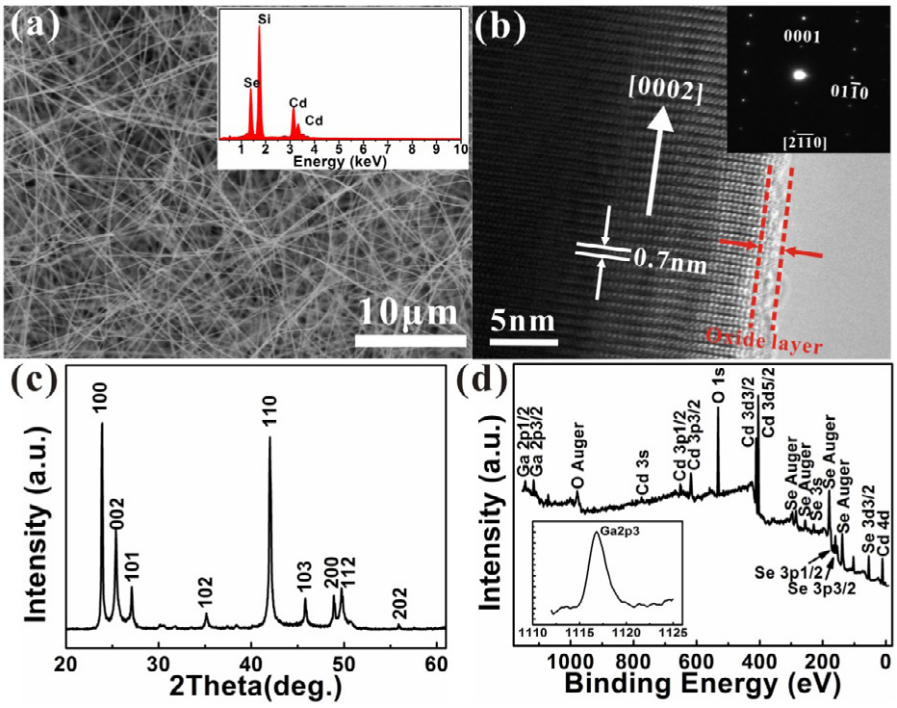

Figure 1. Typical characterization of the Ga doped CdSe NWs. (a) FESEM image, (b) HRTEM image, (c) XRD pattern and (d) XPS spectrum of the as-synthesized CdSe:Ga NWs. The insets in (a), (b) and (d) show the EDX spectrum, corresponding SAED pattern and the enlarged Ga2p3 peak, respectively.

devices. Figure 2(c) shows current–voltage (I–V) curves of an as-synthesized CdSe:Ga NW measured between two In electrodes with dual sweep, which demonstrates the good Ohmic contact between the CdSe:Ga NW and the In electrodes, without hysteresis from the CdSe:Ga NW. Figure 2(d) and its inset depict typical two-terminal I–V curves for a fabricated Schottky barrier diode (SBD) on an individual CdSe:Ga NW with a compliance current of 10^{-4} A on a linear scale and a semilogarithmic scale, respectively. Here the forward bias is defined as a positive bias applied to the Au electrode. The CdSe:Ga NW/Au SBD shows excellent Schottky rectification characteristics with a rectification ratio up to 10^5, implying that excellent Schottky contact is achieved. In addition to the rectifying behavior, obvious resistive switching is also observed when sequential voltage sweeping of -0.5 to $+2$ V and back to -0.5 V is applied. The device exhibits two stable resistance states, a high-resistance state (HRS or OFF) and a low-resistance state (LRS or ON). The current shows a strongly asymmetric shape with a maximum current ratio of $\sim 10^4$ at 0.5 V. When a positive voltage sweep was applied, a SET process from an HRS to an LRS appeared, whereas the application of a negative voltage sweep resulted in a RESET process from an LRS to an HRS. The switching process from an HRS to an LRS and from an LRS to an HRS is illustrated in figure 2(d). After the SET process, the device remains in the LRS and a nonvolatile ON state is achieved; this process can serve to 'write' data into the device. On sweeping again from 2 to -0.5 V, the RESET process occurs, thus the device is changed to the HRS and a nonvolatile OFF state is achieved, which can serve to 'delete' data from the device. It is worth noting that a dual sweep on a single CdSe:Ga NW with Ohmic contact electrodes does not show any visible hysteresis, indicating that the hysteresis does not come from the surface states of the NW. Moreover, additional statistical data for CdSe:Ga NW/Au Schottky memory devices were further obtained by measurements on more than 40 devices. Notably, the devices exhibited a similar electrical switching behavior with abrupt increase and decrease (figure 2(e)), and the histogram summarizing the threshold voltage presented a relatively narrow $V_{\rm th}$ distribution at 0.8–1.2 V, as shown in figure 2(f), indicating the excellent reproducibility of the devices.

The retention performance and switching endurance of the CdSe:Ga NW/Au Schottky memory devices were studied in ambient air at room temperature without any protection, as shown in figures 3(a) and (b), respectively. Pulses of ± 2 V (writing pulse) were applied to switch the resistance state between the HRS and the LRS, which were detected using a small pulse voltage of $+0.5$ V (reading pulse). The reading pulses were repeated to read the resistances of both the HRS and the LRS after either of them was written with -2 V or $+2$ V, respectively. A long retention time of over 10^4 s was obtained for both the LRS and the HRS by consecutive tests, and the HRS/LRS resistance ratio remained at 4×10^4 with only tiny degradation. Moreover, in the storage retention test, which was carried out by reading the resistance state every two months, the HRS was found to be always stable, while the LRS had a tiny increase and was stable. Additionally, it was observed that after eight months the resistance ratio $R_{\rm HRS}/R_{\rm LRS}$ decreased to 3.5×10^4, as shown in the inset of figure 3(a). However, both the HRS and the

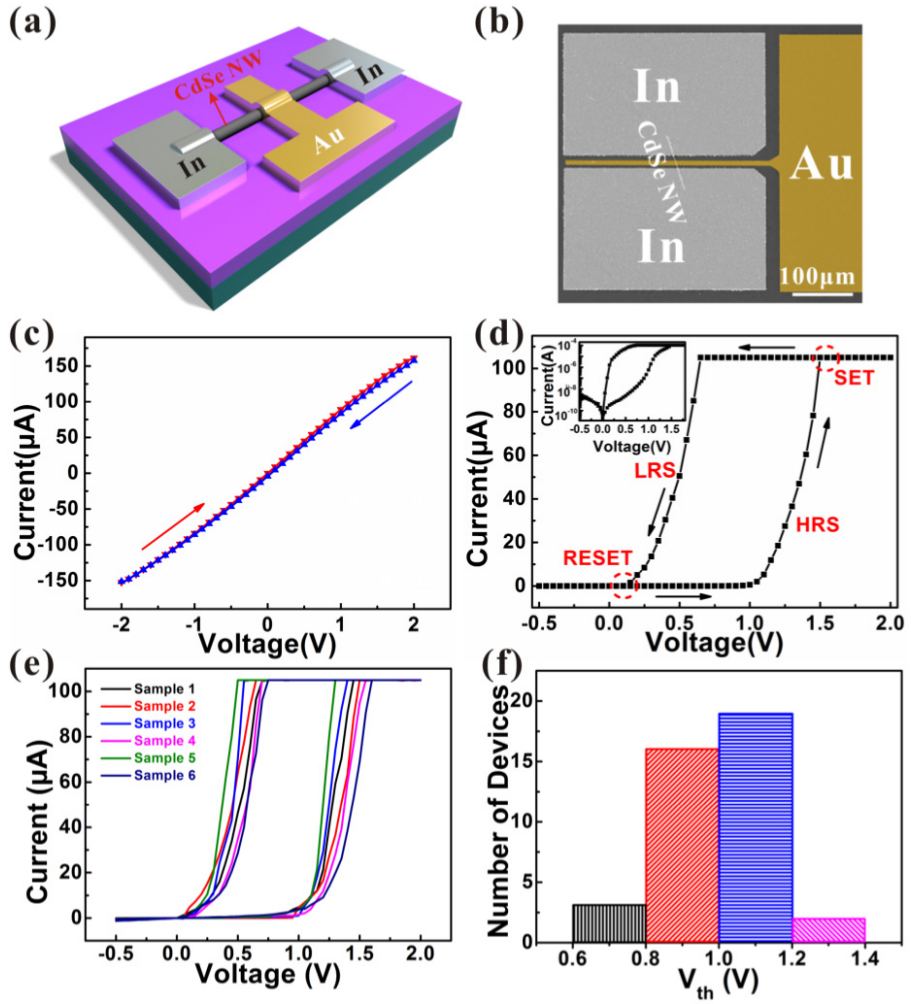

Figure 2. Schematic illustration (a) and SEM image (b) of CdSe:Ga NW/Au Schottky memory. (c) *I–V* curves of a CdSe:Ga NW with a dual sweep. (d) Typical *I–V* curve of a CdSe:Ga NW/Au Schottky diode with huge hysteretic behavior on the linear scale and semilogarithmic scale (inset) measured with a compliance current of 10^{-4} A. (e) *I–V* curves measured from six CdSe:Ga NW/Au Schottky memory devices. (f) Histogram of the threshold voltage distribution from 40 devices.

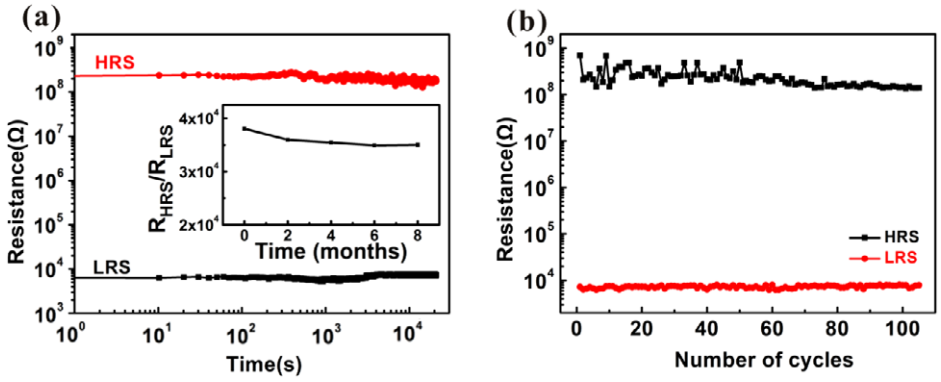

Figure 3. (a) The retention performance of the CdSe:Ga NW/Au Schottky memory device. The inset shows the time dependence of the resistance ratio between the HRS and the LRS. (b) The switching endurance for the first 100 cycles under a read voltage of 0.5 V.

LRS remained stable with no significant resistance change if the time was further increased. The retention measurements indicated that the CdSe:Ga/Au memory devices were stable enough for memory applications. To further demonstrate the reproducibility of the memory, the device was continuously switched between the HRS and the LRS by applying a pulsed voltage for the SET and RESET process. Pulses of ±2 V were applied to switch the resistance state between the HRS

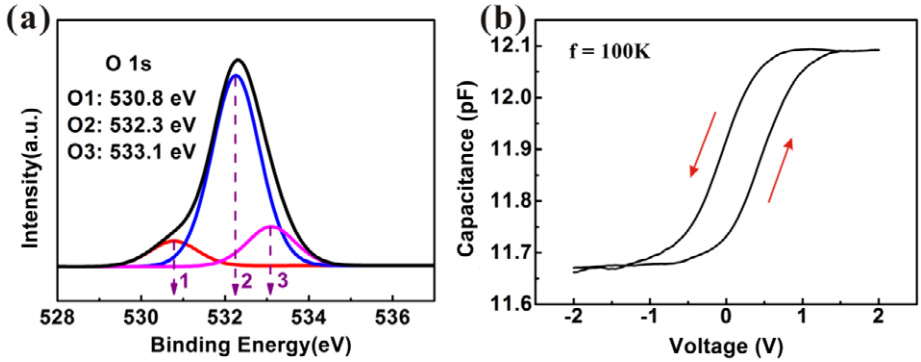

Figure 4. (a) The XPS spectrum of O 1s of as-synthesized CdSe:Ga NWs. (b) The capacitance–voltage curve of a CdSe:Ga NW/Au Schottky memory device measured at a frequency of 100 K.

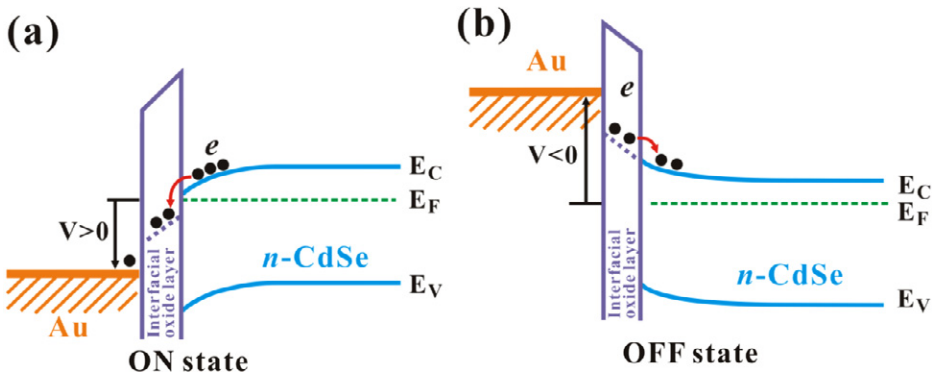

Figure 5. The energy-band diagram of the CdSe:Ga NW/Au Schottky memory in (a) the on state and (b) the off state.

and the LRS, and a small voltage of 0.5 V was applied to read the resistance. The first one hundred cycles for the memory devices are shown in figure 3(b); these demonstrate that the device is stable and rewritable. The long retention and reproducible switching characteristics signify that the CdSe:Ga NW/Au Schottky device is a potentially promising system for memory applications.

Although Schottky interface-related switching has been reported before, direct evidence that shows a clear relationship between the storage characteristics and the interface effect is worthy of further demonstration [10]. In order to understand the unusual switching behavior of the CdSe:Ga NW/Au Schottky memory in this study, HRTEM, XPS and capacitance–voltage (*C*–*V*) measurements were carried out to investigate the surface states of the as-synthesized CdSe:Ga NWs and the Schottky junction, respectively, as shown in figures 1(b) and 4. To verify the surface of a CdSe NW, in the HRTEM characterization (figure 1(b)), a native amorphous oxide layer of 2–3 nm was found on the surface of the crystalline CdSe nanowire, which may play a important role in the hysteresis behavior. In order to verify this point, XPS was carried out to analyze the surface nature of the CdSe NWs at 3–5 nm depth. O 1s can be deconvoluted by three nearly Gaussian curves, centered at 530.8, 532.3 and 533.1 eV, as shown in figure 4(a). The component O2 at 532.3 eV is usually attributed to chemically absorbed O at the surfaces of the CdSe NWs. The component O1 at 530.8 eV is attributed to O^{2-} ions in the native oxidate. The component O3 centered at 533.1 eV is associated with the O vacancies. Furthermore, the *C*–*V* measurement of the CdSe:Ga NW/Au Schottky memory was studied, which can be used for characterization of oxide and interface trapped charges, and oxide thickness [29], as shown in figure 4(b). The *C*–*V* curve was recorded at a high frequency of 100 K with an AC test level of 30 mV by sequential voltage sweeping of −2 to +2 V and back to −2 V. The curve shows an obvious counterclockwise hysteresis behavior which confirms the electron trapping and detrapping processes [30]. The capacitance is maintained at a lower value, increases abruptly and then remains at a high value during the voltage dual sweep between −2 and +2 V, which is quite similar to the behavior observed in metal–insulator–semiconductor (MIS) structures with n-type substrates at a high frequency [31, 32]. It is demonstrated that there is an ultrathin interfacial oxide layer between the CdSe NW and the Au electrode, which serves as the charge storage medium [29, 33]. When a voltage sweep from −2 to +2 V is applied, electrons can be trapped into the interfacial oxide layer. The captured electrons can generate an internal electric field along the direction of the applied voltage, giving rise to a increased capacitance. In contrast, when a reverse sweep is made from +2 to −2 V, electrons in the interfacial oxide layer are detrapped, leading to a decrease of the capacitance value.

In light of the above structural characterization, the principle of the CdSe:Ga NW/Au Schottky memory can be easily understood from the energy-band diagram depicted in figure 5. The interfacial oxide layer at the junction interface

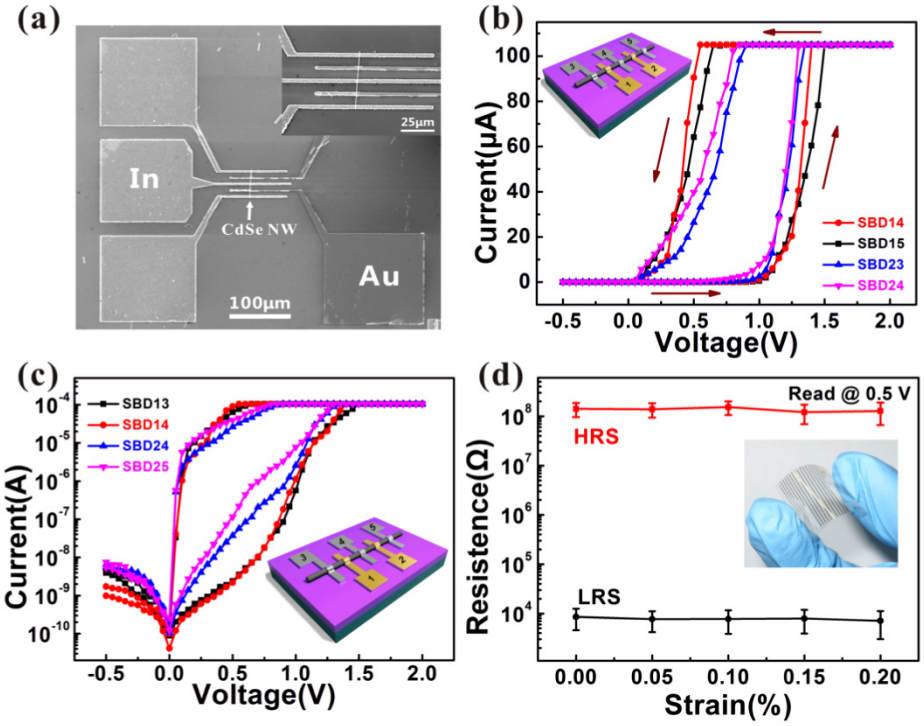

Figure 6. (a) An SEM image of a multibit CdSe:Ga NW/Au Schottky memory device. (b) *I–V* curves of the memory device with varying Schottky/Ohmic contact distances. (c) *I–V* curves of the multibit memory device on a semilogarithmic scale. (d) The resistance ratio between the HRS and the LRS as a function of surface strain. The inset is a photograph of a flexible memory device made on a PET substrate.

makes the device function like a floating gate memory. The oxygen vacancies resulting from the partial oxidation can serve as the trapping centers for electrons. Under the forward bias, electrons from the CdSe NW are injected into the interfacial oxide layer and trapped by oxygen vacancies in the interfacial oxide layer [3, 5]. This process reduces the Schottky barrier height and leads to the ON state (LRS) of the memory (figure 5(a)). This corresponds to a write operation for the memory. On the contrary, under reverse bias, electrons trapped by oxygen vacancies in the interfacial oxide layer will be injected into the CdSe NW, leading to an increase of the barrier height, which will lead to the OFF state (HRS) for the memory, corresponding to an erase operation for the memory (figure 5(b)).

To achieve high-density memory, it is crucial to reduce the size of the memory cells. Multibit storage ability of Schottky memory based on an individual CdSe:Ga NW will offer the capability of reducing the size of the memory cell. The number of Schottky electrodes made on a nanowire will determine the number of bytes for each nanowire. Therefore, multibit memory can be achieved by integrating several SBDs on an individual nanowire. In this work, a memory of two bits was fabricated as shown in figure 6(a). Two Au electrodes and three In electrodes were fabricated on an individual CdSe:Ga NW, marked as 1, 2, 3, 4 and 5, respectively, including two independent SBDs for a two-bit memory device. First, *I–V* curves of Schottky memory devices with varying distance between the Schottky and Ohmic electrodes are shown in figure 6(b). The *I–V* curves of SBD14 (between electrodes 1 and 4) and SBD15 are not very different, and the same result was observed from SBD23 and SBD24, indicating that the distance between the Schottky and Ohmic electrodes has no obvious effect on the memory device. Figure 6(c) depicts *I–V* curves of four CdSe:Ga NW/Au SBDs (SBD13, SBD14, SBD24 and SBD25) on the semilogarithmic scale, which show excellent Schottky rectification characteristics and obvious hysteresis behavior. The measurements on the four SBDs exhibit similar results, indicating the good reproducibility and stability of the CdSe:Ga NW/Au Schottky memory devices. The ability to store multibit information in a single NW enables a nonvolatile memory device with ultrahigh integration density to be achieved.

Flexible devices have attracted great interest due to their advantages in future applications over conventional bulk silicon technology [34, 35]. The remarkable mechanical properties of one-dimensional nanostructures have attracted much attention in terms of their potential applications in flexible and transparent optoelectronics [36–39]. Here, we conduct a primary study on flexible memories based on CdSe:Ga NWs by using poly ethylene terephthalate (PET) flexible and transparent substrate instead of the SiO_2/Si substrate. The CdSe:Ga NW/Au Schottky memory devices show excellent mechanical properties in bending test results as a function of surface strain (figure 6(d)). The ON and OFF states were measured at a read voltage of 0.5 V at each bending angle. For surface strain values ranging from 0% to 0.2%, there were negligible changes in the resistance values of the ON and OFF states, revealing the excellent stability of the flexible memory device. These results confirm that the CdSe:Ga NW/Au Schottky memory devices exhibit excellent

mechanical flexibility as well as good memory properties, revealing their suitability for flexible transparent electronic device applications.

4. Conclusions

In summary, nonvolatile multibit resistance switching memory devices based on CdSe:Ga NW/Au SBDs have been demonstrated. The devices show high performance of their storage characteristics such as their high-resistance on/off ratio, long retention time and low operating voltage. The underlying mechanisms of CdSe:Ga NW/Au SBD RS memory are well described and understood by electrons trapping and detrapping in the interfacial oxide layer. Moreover, flexible and transparent memory devices based on CdSe:Ga nanoSBD structure have also been demonstrated, which will have potential application for next-generation high-density and high-performance nonvolatile memory.

Acknowledgments

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